Combined Digital/Wireless Link over the Multi-Mode Fiber with VCSEL using CMOS based Feedforward Equalizer

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Combined Digital/Wireless Link over the Multi-Mode Fiber with VCSEL using CMOS based Feedforward Equalizer

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SUMMARY

In this dissertation, the combined optical link, where the baseband digital signal and wireless signal are transmitted simultaneously over a multi-mode fiber (MMF) using an VCSEL and received through a photoreceiver and a feed forward equalizer (FFE). For this hybrid optical link, a new type of combiner is developed using the multi-layer organic (MLO) process. For the overall link simulation, a rate-equation-based VCSEL model is developed with circuit components. This model describes the high-speed modulation characteristic as well as the thermal effect on the L-I (light vs. bias current) characteristic.

Additionally, The FFE is developed to further extend a MMF distance by compensating differential modal delay (DMD) in MMF. Two different implementation approaches are taken for the FFE by passive LC ladder based delay line and active inductance peaking delay line structure. To overcome the voltage headroom limitation of the conventional Gilbert cell architecture, modified Gilbert cell is presented and implemented as a multiplier cell for both FFEs. The FFEs are fully integrated on a single chip and fabricated by a standard 0.18 μm CMOS process. The developed FFE successfully rebuild the distorted signal form the MMF at 10 Gbps data rate.

CHAPTER I

INTRODUCTION

With the explosion of the information age and the increased demands for data services such as the Internet, e-commerce, telecommuting, and home-office expansion, the need for various wire/wireless/fiber-optic data communication systems has arrived. For short-reach applications, current systems consist of copper cables and optical fiber channel, but for the future bandwidth expansion, optical fiber will be deployed widely over copper cables because of the intrinsic broad bandwidth characteristics. Eventhough the optical fiber has broadband characteristic over copper cables, it is not yet used with their full capacity because of several dispersion effect on the signal. One solution to this efficiency problem is to employ a hybrid approach, which can seamlessly integrate multi-band signals [2] One of the promising system example is the short reach combined digital/wireless fiber optic link, which transmits baseband signals and wireless signals such as global system for mobile communications (GSM)/personal communications services (PCS)/wireless local area network (WLAN) data traffic simultaneously via a fiber-optic link [2]. The brief history for the simultaneous transmission of baseband and wireless signals scheme is written in the following section.

The first four-channel optical subcarrier multiplexing (OSCM) transmitter module based on monolithic microwave integrated circuit (MMIC) is presented in [3]. The module consists of one MMIC and four coupled line bandpass filters. The developed module generates four subcarrier signals with 500 MHz spacing and supports up to 50

Mbps of non-return-to-zero (NRZ) data. The designed integrated circuit (IC) consists of four voltage controlled oscillators (VCOs), which can cover a frequency range of 3.8-5.5 GHz for subcarrier signal generation. The author shows first the feasibility of an IC implementation for the subcarrier signal generation.

In 2001, *Kamisaka et al*. show the experimental demonstration for the simultaneous transmission of the baseband signal and subcarrier signal through the electro-absorption modulator (EAM) [4]. The 10 Gbps NRZ baseband signal is transmitted simultaneously with a 155.52 Mbps differential-phase-shift-keying (DPSK) modulated subcarrier signal at 60 GHz. The nonlinear effect of the EAM is theoretically investigated and the signal distortion resulting from the undesired nonlinearity of the EAM is numerically clarified. However, further implementation as a transmitter module is still required.

Apart from this experimental demonstration, the subcarrier multiplexing scheme is newly proposed for a broadband internet access [5]. For example, in current in-building wireless network such as fiber optic distributed antenna system (DAS), the data is sent through the optical fiber in baseband and the data is modulated and up-converted to radio frequency at radio access node (RAN) for wireless end users. However, this multi-functionality of RAN makes it cumbersome for its circuit complexity and cost. To ameliorate this issue, a new data transmission method is proposed where the RAN receives the modulated and up-converted radio frequency (RF) signal through the optical fiber and transmits it directly through the antenna with proper gain [5]. At the same time, the baseband signal is transmitted simultaneously through the optical fiber for a wired network. In this way, the RAN functionality can be simplified. The authors in [5] show

the overall system concept and the analysis regarding the nonlinearity of the optical source. However the overall system is not implemented.

In the evolution of the OSCM to different applications, one promising system is the short reach combined digital/wireless fiber optic link, which transmits baseband Ethernet signals and RF signals for GSM/PCS/WLAN data traffic simultaneously via a fiber-optic link [2]. Figure 1.1 shows one example of the hybrid optical network.

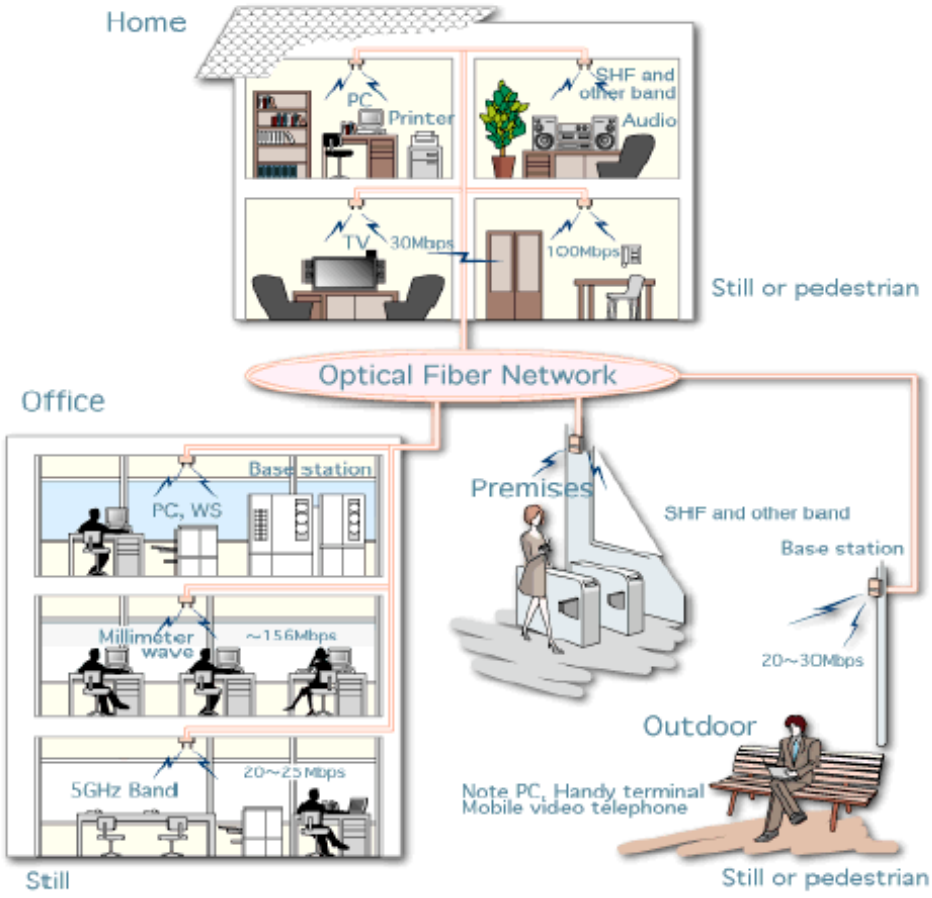


Figure 1.1. Example of the hybrid optical link.

In this dissertation, combined digital/wireless fiber optic link is studied, where a vertical-cavity-surface-emitting-laser (VCSEL) is used as the light source with a multi-mode fiber (MMF) as a channel. The MMF channel has undesirable dispersion effect on the signal such as differential modal delay (DMD) as the fiber length is increased. To extend the distance of the MMF for the combined digital/wireless fiber optic link, a complementary metal oxide semiconductor (CMOS) based feedforward equalizer (FFE) is also developed. The FFE compensates the DMD dispersion in the MMF resulting in further extension of the MMF distance.

To compensate the signal impairment in fiber channel, several approaches have been published so far. Most of the compensation technique is researched in pure optical domain such as using dispersion-compensation fiber, adaptively tuned birefringence or offset launching from the light source to the fiber. However the optical approaches to compensate the dispersions in fiber is still very bulky and expensive solution. Therefore it is desirable to use the advanced signal processing technique to compensate any signal impairments in the electrical domain. The electrical equalization is already being used in the copper channel to compensate the inter-symbol-interference (ISI) caused by the signal impairment from the frequency dependent channel loss characteristics, echo, and channel interference from the adjacent channel. Recently, the electrical equalizer is reported for fiber optic application as well [6].

In this dissertation, the background knowledge for the equalization and the history of fiber dispersion compensation in optical and electrical domain approaches are studied. From the literature survey of various type of equalizer implementation method, finite impulse response (FIR) type of equalizer is selected for fiber dispersion compensation.

The system level equalizer simulation is performed for the given MMF channel and the optimum system specification is extracted. Finally, the equalizer is implemented on a single IC using 0.18 um CMOS technology with two different implementation approaches. Both of the equalizer IC is designed and tested with the 500 m length MMF by transmitting and receiving the NRZ data successfully up to 10 Gbps data through put.

The original contributions of this dissertation include:

1. Development of the novel combiner, which is first in its scheme for fiber-optic applications.

2. First module development for combined digital/wireless communication over MMF via VCSEL with direct modulation method.

3. First continuous time FFE with 0.18um CMOS technology for 10 Gbps data through put over MMF.

This dissertation is organized as follows:

In chapter 1, brief historical background of the simultaneous transmission over fiber and the organization of the dissertation is described. In chapter 2, combined digital/wireless link over MMF is described in detail. The hybrid combiner development procedure for this combined optical link is described in detail. Design of the combiner over multi-layer organic (MLO) process is shown with the S-parameter measurement results. Also the VCSEL characteristic and model development procedure is described in this chapter. The VCSEL model is developed based on the well-known rate equation to enable 2 port model. The empirical model is composed of several lumped element circuit blocks to implement rate equation. Finally the chapter 2 shows the overall combined link measurement result.

Chapter 3 describes the equalizer design. The various types of dispersion in fiber are described with its effect on fiber communication system. The technical solutions to resolve these issues are introduced from the optical domain efforts to electrical domain approaches. Also various types of equalizers are presented from the system level configuration to the IC level implementation. Chapter 4 focuses on the equalizer design with passive LC artificial transmission line implementation. The MMF channel is characterized by S-parameter measurements. The measured frequency dependent loss characteristic of the channel is used to extract the optimum equalizer specification such as the number of tap, tap coefficients, and tap delay amount. The overall equalizer configuration, design procedure, and transistor level building block is described in this chapter. The simulation and measurement result of this equalizer to compensate DMD in 500 m of MMF at 10 Gbps data through put is shown as well. The chapter 5 describes the equalizer design with active delay line structure. The overall pros and cons of the passive delay line and the active delay line approaches are described. The equalizer configuration, IC implementation, and building blocks are described in detail. Finally, the conclusion is in the chapter 6.

CHAPTER II

COMBINED DIGITAL/WIRELESS LINK WITH VCSEL

In this chapter, the detailed work for the combined digital/wireless link with MMF over VCSEL is described. All the work is organized as follow: 1) overall combined optical link configuration, 2) the detailed description of the developed combiner, 3) VCSEL characteristic and model, 4) combined optical link measurement result. On the combiner section, the design procedure, an implementation, and the measurement results are shown. In the VCSEL model section, the VCSEL characterization procedure is presented with the DC-IV and high frequency measurement setup. Also, the model development procedure and verification with measurement results are shown. Finally, the measurement results of the combined digital/wireless link over the MMF are shown with the overall simulation results.

2.1 COMBINED DIGITAL/WIRELESS LINK CONFIGURATION

The overall hybrid optical link is composed of an improved broadband combiner, a VCSEL with 10 GHz modulation bandwidth, a photoreceiver, and a splitter that separates the baseband signal from the WLAN signal in the receiver. The basic block diagram of the overall hybrid optical link is shown in Figure 2.1. The baseband digital signal (OC-

48) and the WLAN signal (802.11a), which is at 5.8 GHz, are sent through the combiner, which is implemented on a MLO board. The combined baseband and WLAN signal is transmitted over a 100 m MMF with 50 μm core size. The signals are transmitted with a 10 GHz VCSEL, which is mounted on the MLO board and wire-bonded to the combiner.

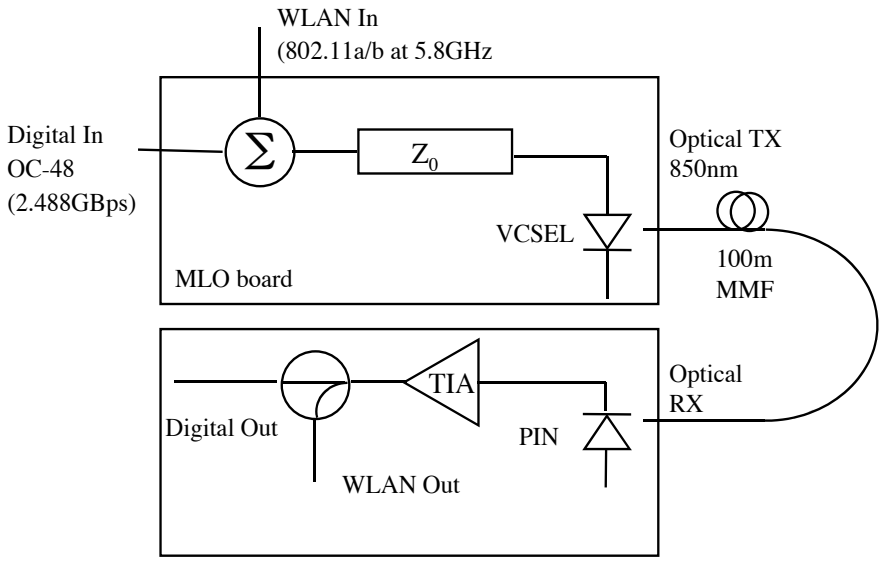


Figure 2.1. Basic block diagram of the hybrid optical link.

2.2 COMBINER DEVELOPMENT

A novel combiner is developed for the hybrid optical link. The combiner successfully combines the digital baseband signal and modulated RF signal without distorting the digital baseband signal. This combiner can selectively couple the RF spectrum by changing the design parameter, so that we can optimize the coupling efficiency at the desired frequency band. As a practical implementation, the combiner is designed with two different operating frequencies. First, the combiner is designed for a hybrid optical link, where an OC-48 (2.488 Gbps) data stream and an 802.11a wireless signal at 5.8 GHz are combined. Also, the other combiner is designed mainly for the OSCM module, where a 7 Gbps pseudo random bit sequence (PRBS) baseband signal is simultaneously transmitted with the subcarrier signal at 14 GHz. A detailed design procedure is presented in the combiner design section.

2.2.1 COMBINER BRIEF INTRODUCTION

For the implementation of the combined digital/wireless optical link, a device that can combine the digital baseband signal and wireless signal with reliable insertion loss and isolation in both bands is essential. The conventional Wilkinson power combiner is not suitable for broadband applications as it needs more multiple sections and increases overall insertion loss and circuit complexity [7]. Many efforts have been made to develop a broadband coupling structure, such as the wide-band uniplanar magic-T [8] and broadband rat-race ring coupler [9]. However, those broadband devices are not

appropriate for this combined digital/wireless optical link. Because those are basically ac coupling structure with certain center frequency, the signal using those devices experiences severe signal loss around the baseband region. As a result, a different type of combiner is required to implement the combined optical link. In this dissertation, we present a new type of combiner that can combine the digital baseband signal and wireless signal with proper insertion loss and isolation [10]. The combiner is composed of a low pass filter (LPF) and a vertical coupling structure, which is developed by modifying the conventional coupled line coupler. The detailed design procedure and measurement results are presented in the following section

2.2.2 COMBINER DESIGN AND IMPLEMENTATION

The combiner has the capability to combine the modulated wireless signal with the baseband data stream. This multi-layer structure is composed of three parts. As seen from Figure 2.2, the baseband signal flows through a step-impedance LPF, embedded microstrip line, and vertical coupling structure. For the combined digital/wireless optical link, the input port of the LPF (port 1 in Figure 2.2) works for the baseband digital data stream. Port 2 in Figure 2.2 is used for the modulated RF signal, such as the 14 GHz subcarrier signal and 802.11a WLAN signal.

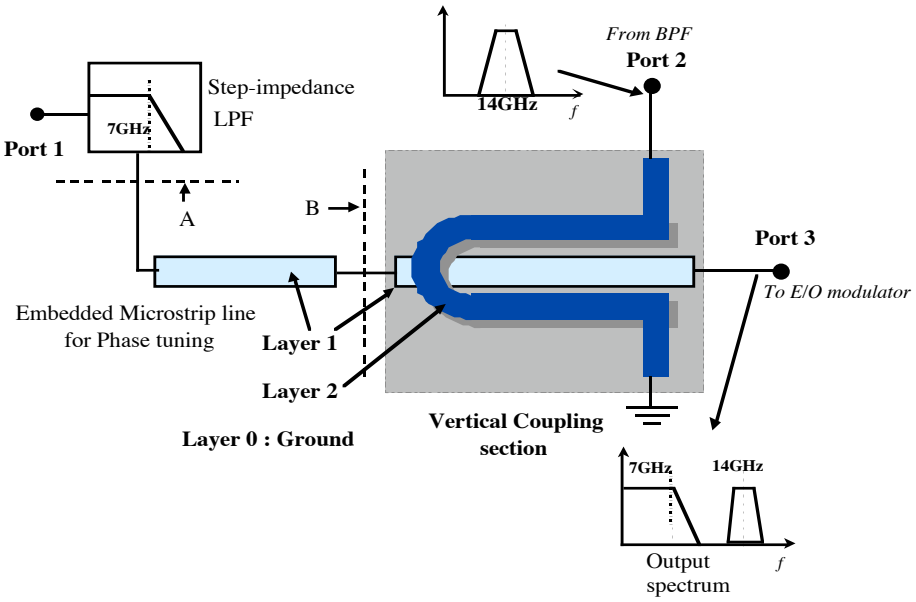


Figure 2.2. Schematic of the combiner (for OSCM module).

To overcome the disadvantage of the conventional combiner, we modified the conventional coupled line coupler as a vertical coupling structure, as shown in Figure 2.3. The output port of the coupled line coupler is used as the input port for the wireless signal and the isolation port is shorted to the ground. Also, we designed ninth-order Bessel LPF at the input port for the baseband, which performs as a band stop filter for the RF signal and reflects the RF signal at the output of the LPF (reference plane A in Figure 2.2). The embedded microstrip line length, which interconnects the LPF and vertical coupling structure, is optimized to obtain a constructive effect between the reflected RF signal from the LPF output and the signal directly traveling from port 2 to port 3 at the output port of the combiner. The design is finalized with the three-dimensional (3D) method of momentum electromagnetic simulation software [11].

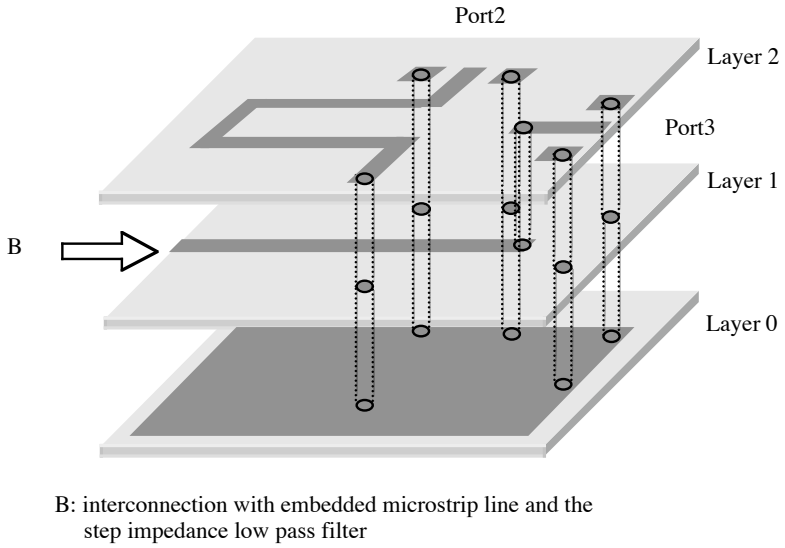
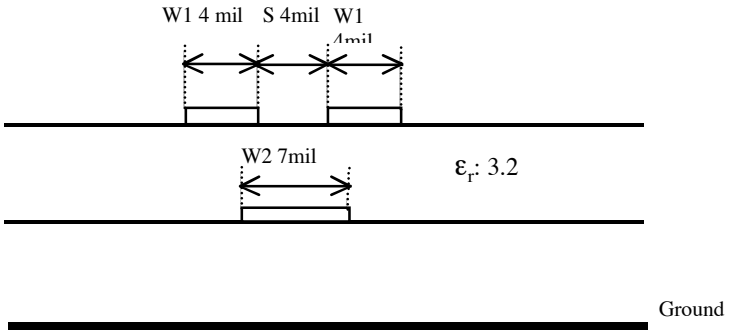


Figure 2.3. Vertical coupling structure in multi-layer organic board.

The designed combiner is fabricated via a MLO process developed in the Georgia Institute of Technology Packaging Research Center (PRC). Three conductor layers are used, and the bottom layer serves as a ground layer. Copper is used as the conductor layer in this process. The dielectric material thickness between all the conductor layers is 2.46 mil, as shown in Figure 2.4. All the conductor layer thicknesses are 9 μm. The top conductor layer is vertically coupled with the embedded transmission line section. The embedded transmission line connected to the output port (port 3 in Figure 2.3) of the combiner through the via. One end of the top conductor layer is used as the RF signal input port, which is port 2 in Figure 2.3. The other end of the top conductor layer structure is shorted to ground, as shown in Figure 2.3. The width of the top conductor layer and bottom conductor layer is carefully chosen as 4 mil and 7 mil respectively, to optimize the coupling. Figure 2.5 shows the fabricated combiner for the OSCM. The

designed ninth-order Bessel LPF is cofabricated with the vertical coupling structure interconnected via an embedded microstrip line.



W1: top conductor layer width
W2: middle conductor layer width
S: space between the top conductor layers
ε_r:dielectric constant of the organic material

Figure 2.4. Cross section view of the vertical coupling structure.

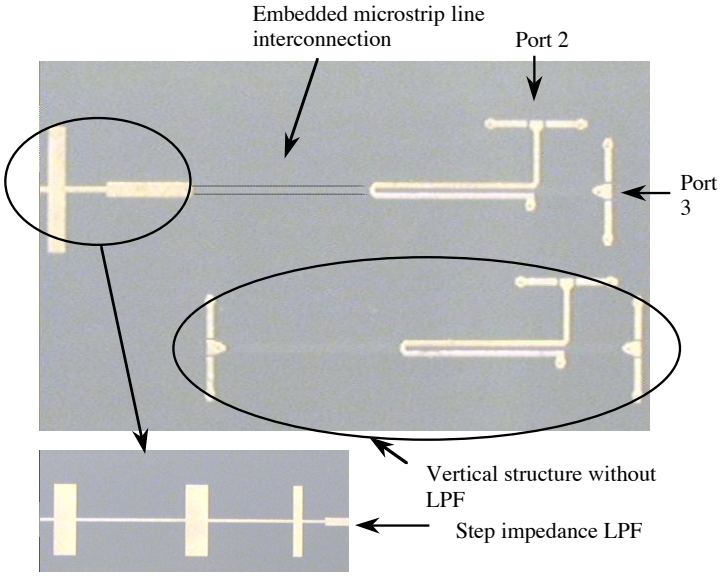


Figure 2.5. Fabricated combiner for OSCM in MLO process.

2.2.3 COMBINER MEASUREMENT RESULT

The HP8510 vector network analyzer (VNA) is used to measure the frequency characteristic of the combiner. Figure 2.6 shows the measurement result of the combiner, which is designed for a combined optical link. Port 1 is used for the baseband signal input, port 2 is used for the WLAN signal, and port 3 is used as the output of the combiner. The insertion loss from port 2 to the output of the combiner was measured to be 1.4 dB. The isolation between port 1 and port 2 of the combiner is greater than 10.6 dB for the baseband signal and 38 dB for the WLAN signal at 5.8 GHz. These results satisfy the requirement for the hybrid optical link.

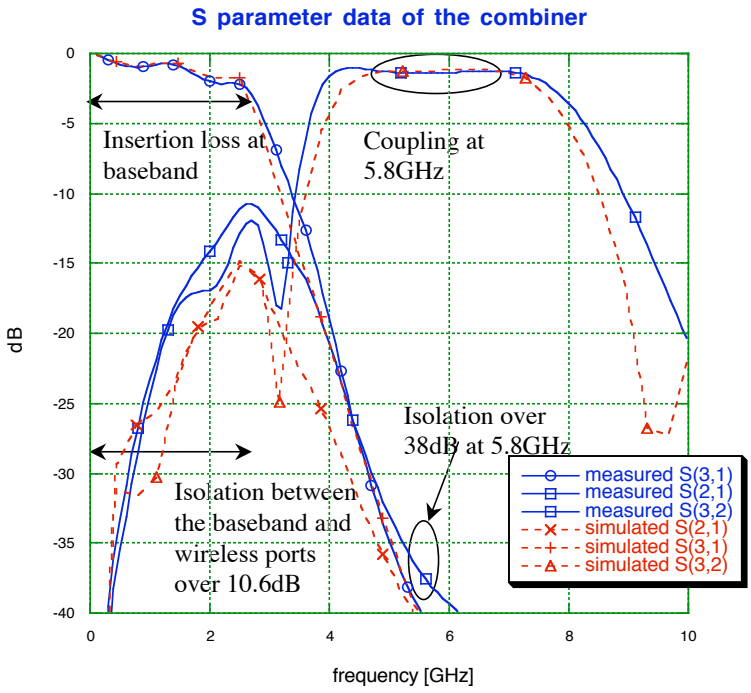


Figure 2.6. Measurement result of the combiner for the hybrid optical link.

Figure 2.7 shows the measurement result of the combiner, which is designed for the OSCM module. The insertion loss of the RF signal at the output port of the combiner is

measured as 1.9 dB. The isolation between port 1 and port 2 of the combiner is greater than 10 dB in baseband and 38 dB at 14 GHz, as shown in Figure 2.7. These results satisfy the requirement for OSCM module. A 3 dB bandwidth of 7 GHz is achieved between port 1 and port 3. Figure 2.8 (a) shows the measured frequency spectrum at the output of the combiner when 7 Gbs PRBS with a 14 GHz sinusoidal wave are sent. Figure 2.8 (b) shows the measured eye opening of the 7 Gbs PRBS at the output port.

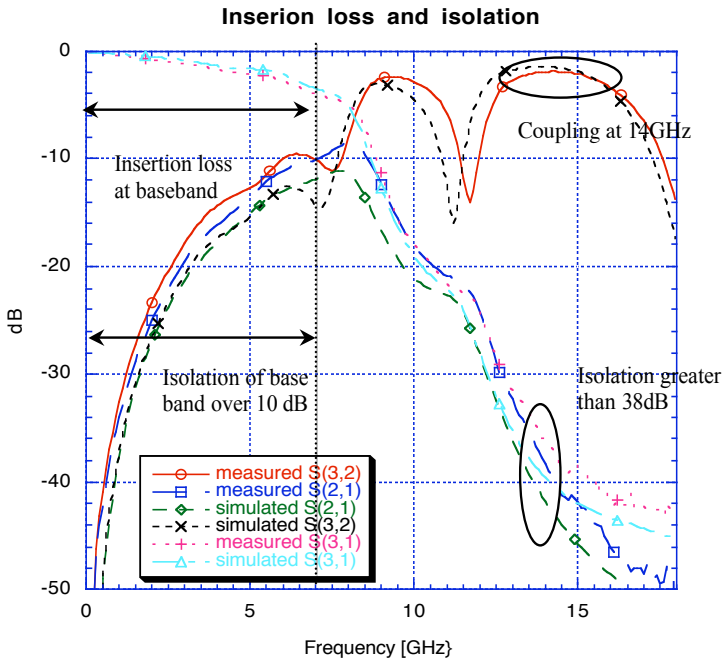
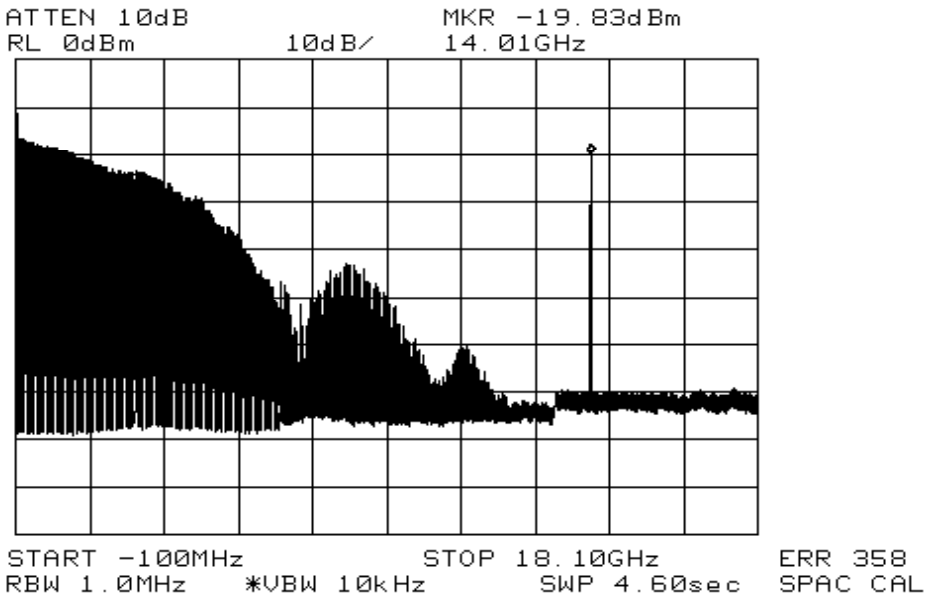
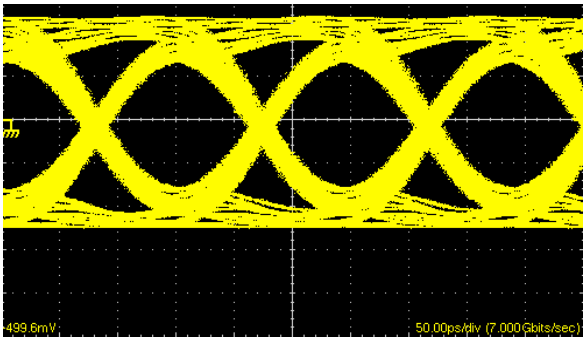


Figure 2.7. Measurement result of the combiner for the OSCM.



(a)



(b)

Figure 2.8. Spectrum and eye diagram of the combined signal after the combiner. (a) Spectrum of the combined signal at the combiner output. (b) Eye diagram of the 7 Gbps PRBS without RF signal transmission.

2.3 VCSEL CHARACTERISTIC AND MODEL

For the perspective of the optoelectronic circuit design, the VCSEL model is essential for optimizing the driver circuitry. Contemporary circuit designs use a simple RC parallel lumped element VCSEL model. However, for the overall system-level simulation and prediction of the modulated optical signal waveform, a two-port model of the VCSEL is necessary. In this dissertation, the developed VCSEL model is studied, which can describe the optical power intensity vs. the injection current (L-I), including thermal roll-over in optical power, input impedance, and the forward transmission characteristic of the VCSEL up to 15 GHz. The brief introduction section will cover the general background of the VCSEL and the demands for the VCSEL model. The following section describes the VCSEL measurement characteristics. Finally, the VCSEL model development procedure is written on the section 2.3.3.

2.3.1 VCSEL INTRODUCTION

VCSELs have been the subject of many research efforts because of several promises such as inexpensiveness, low-threshold voltage, and high-speed modulation characteristic for optical communication systems. The advantage of the VCSEL over the conventional edge-emitting laser is that hundreds of VCSELs can be integrated on a single wafer with great uniformity.

In this dissertation, the main advantage of the VCSEL is reviewed from two different points of view: manufacturing point of view and performance point of view. From the

manufacturing point of view, each VCSEL element on the two-dimensional array can be tested on a wafer level [12], differentiating it from the edge-emitting laser, which needs to be cleaved to bars and tested individually. Also, the circular beam forming and small numerical aperture of the VCSEL make it easier to couple with fiber [13]. The easy extension of the VCSEL element to a two-dimensional array offers the possibility of fiber bundle applications [12]. From the performance point of view, a small active region of the VCSEL allows for low threshold current operation. In addition, the small active region provides higher modulation bandwidth than other types of laser with equivalent output power. This is due to higher photon densities reducing radiative lifetime [14].

Despite these advantages of the VCSEL, it still has some less desirable features. For example, multimode operation is possible because of the existence of higher-order transverse modes [15]. Also, the spatial hole burning can limit the VCSEL performance by contributing to mode competition [16]. However, the most significant factor that limits the VCSEL performance is the thermal dependence of the VCSEL, owing to the poor heat dissipation and large resistance introduced by distributed Bragg Reflectors [17]. The threshold current of the VCSEL can be varied with different operating temperature. Also, the light-current (L-I) characteristic depends on the temperature. As the injection current increases, the device temperature increases and the VCSEL output power starts to saturate and roll over [18].

To address the thermal behavior of the VCSEL, several models have been proposed. However, most of them use numerical modeling through multi-dimensional analysis [19]. Eventhough the numerical model can describe accurate performance of the VCSEL, the empirical model can be used easily in CAD tools for design performance. Also, from the

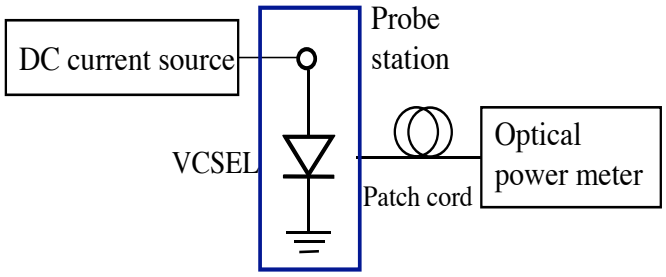
opto-electronic (OE) circuit design perspective, the circuit-based temperature-dependent VCSEL model is highly required.

The circuit component-based temperature-dependent VCSEL model has been proposed previously [20]. In [20], the input impedance characteristic is measured with a network analyzer up to 15 GHz on various temperatures, and a one-port input impedance characteristic model is implemented using temperature-dependent coefficient parameters. However, the forward transmission characteristic of the VCSEL is still required to be properly modeled for an optical link system design. In [21, 22], a complete two-port-based temperature-dependent VCSEL model is proposed. The VCSEL output power roll-over characteristic is properly modeled via the introduction of the offset current. The offset current is modeled as a polynomial equation of the device temperature. Also, based on the rate equation, the forward transmission characteristic of the VCSEL is modeled. However, it still needs the transient temperature differential equation with proper extraction of the VCSEL's thermal resistance. In addition, the offset current polynomial equation relating device temperature is not straightforward to extract. In this dissertation, the two-port based VCSEL model is described with the introduction of the offset current, which is a function of the injection current, so the extraction of the polynomial coefficient is simplified. A detailed measurement procedure of the VCSEL and the measurement characteristics are presented in the following section.

2.3.2 VCSEL MEASUREMENT CHARACTERISTIC

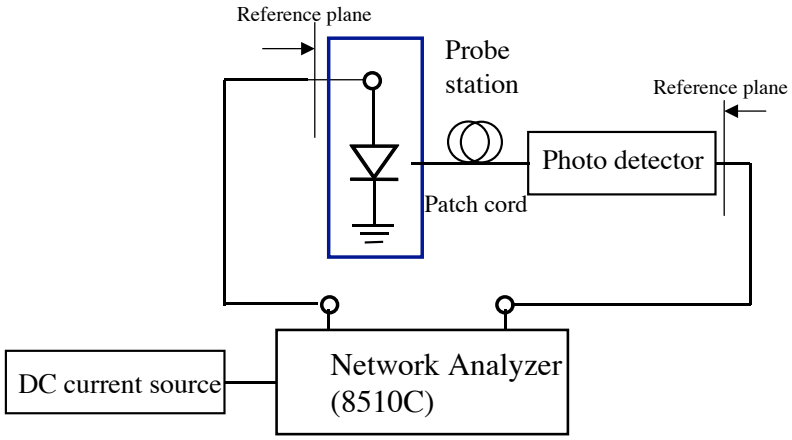
The VCSEL is measured for the L-I characteristic, high-frequency characteristic, and temperature-dependent characteristic. Figure 2.9 shows the setup for the L-I

characteristic and high-frequency characteristic. A 4 X 1 VCSEL array is measured with a fiber alignment kit to minimize the coupling loss. Currently, a calibration method for the optical device measurement is not available, so we set the reference plane on the input port of the VCSEL and the output port of the photo detector via the standard electrical calibration procedure [20]. To measure the VCSEL high-frequency performance correctly, the photodetector is guaranteed for a higher modulation bandwidth compared with measured VCSEL. Also, the DC current is biased to the VCSEL through the network analyzer. In addition to the room temperature measurement, the VCSEL measurement with different ambient temperature is performed. Temperature-dependent VCSEL measurement setup is identical to the previous measurement setup except for the use of a thermal chuck under the bare VCSEL.



(a)

Figure 2.9. VCSEL on-wafer measurement setup. (a) L-I characteristic measurement setup. (b) S-parameter measurement setup



(b)

Figure 2.9. Continued

The L-I-V (light power - bias current - voltage) characteristic of the VCSEL at room temperature is shown in Figure 2.10. The VCSEL bias voltage and the output light power are measured via increasing bias current from 0 mA to 14 mA. The light output power is measured at 850 nm light wavelength. The VCSEL light power starts to saturate as the bias current is increased because of the increase of the device temperature. Figure 2.11 shows the L-I characteristic with different temperature conditions. As the ambient temperature increases, the light output power starts to attenuate. Also, the threshold current of the VCSEL starts to increase as the temperature rises. Figure 2.12 shows the temperature - threshold current characteristic.

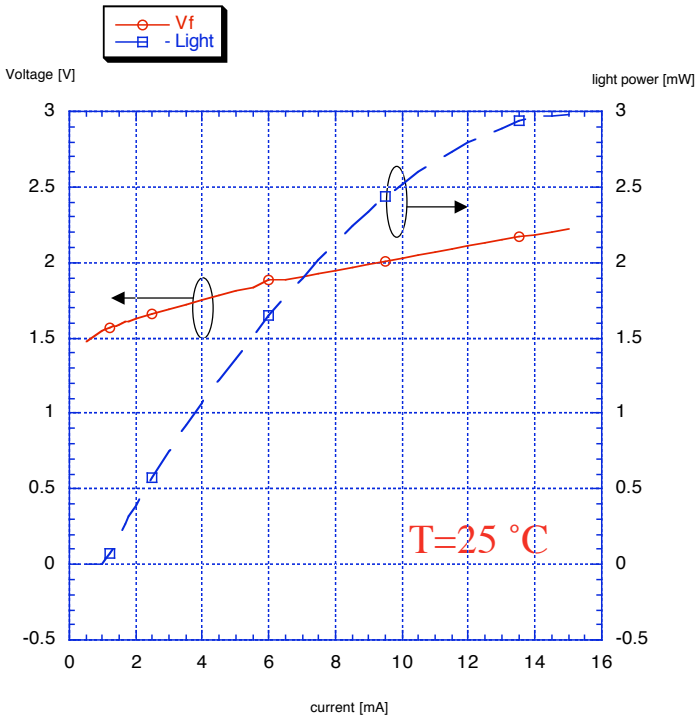


Figure 2.10. VCSEL L-I-V measurement at 25 °C.

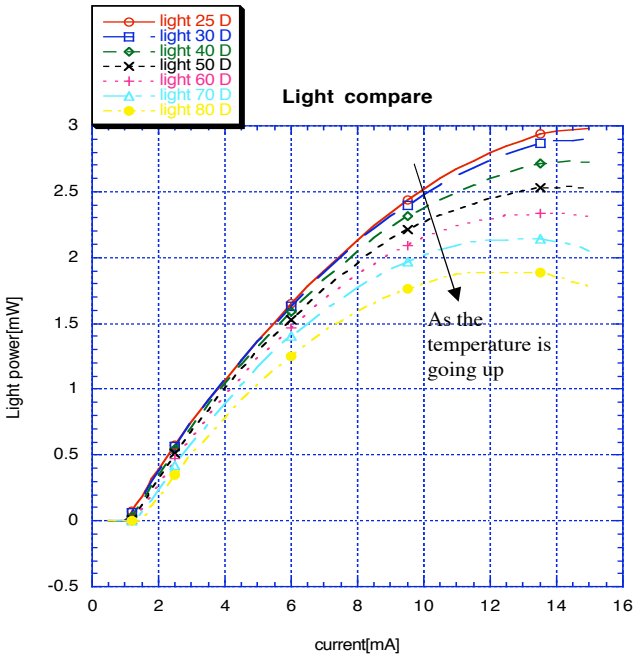


Figure 2.11. VCSEL L-I characteristic with different temperature condition.

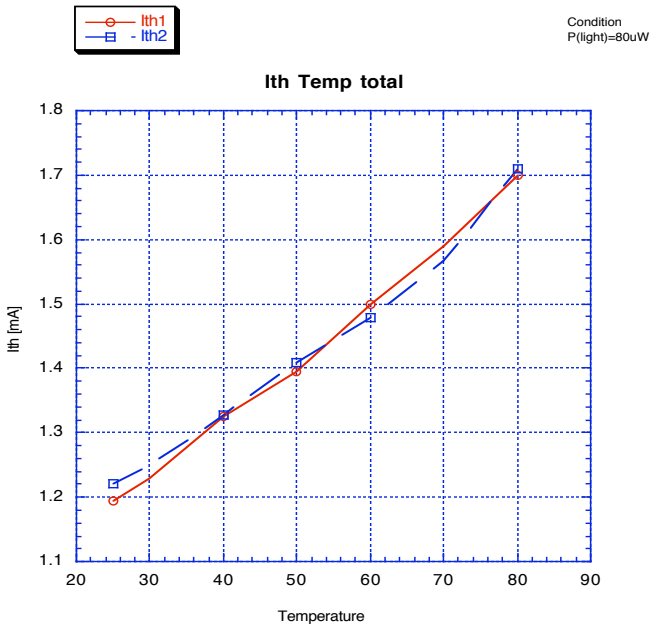


Figure 2.12. Threshold current vs. temperature.

Figure 2.13 shows the I-V characteristic of the VCSEL with different ambient temperature conditions. Differential resistance, $\frac{dV}{dI}$ starts to decrease as the temperature increases. Also, the slope efficiency $\frac{dL}{dI}$ decreases as the temperature is increased.

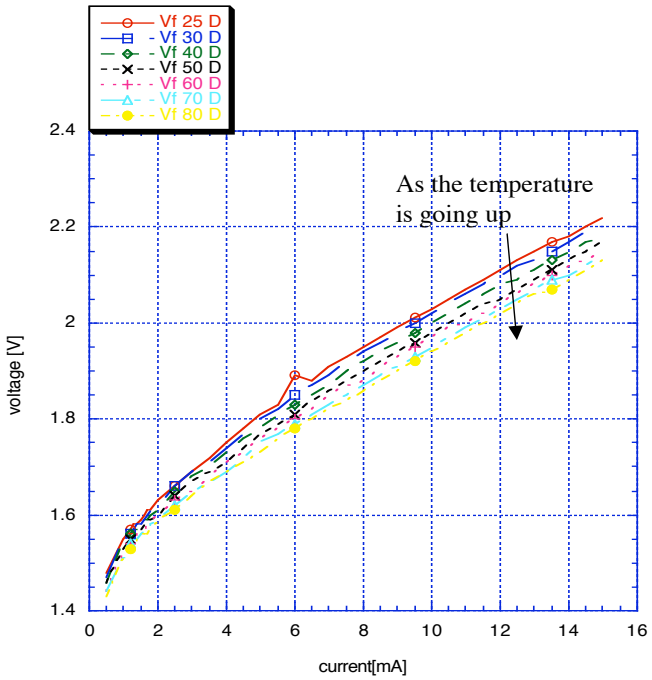


Figure 2.13. VCSEL I-V measurement with different temperature condition.

The VCSEL small-signal characteristic is also measured up to 15-GHz via the setup in Figure 2.9 (b). Figure 2.14 shows the small-signal input reflection characteristic at different bias conditions. At low-frequency range, the VCSEL input impedance is around 50 ohm and goes more capacitive at higher frequency ranges. Also, as the bias current is increased, input resistance at the DC starts to decrease.

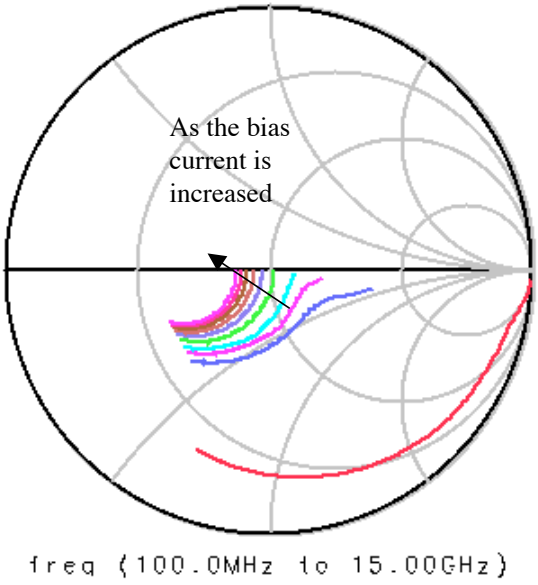


Figure 2.14. Input reflection characteristic (Ibias=1 mA to 15 mA).

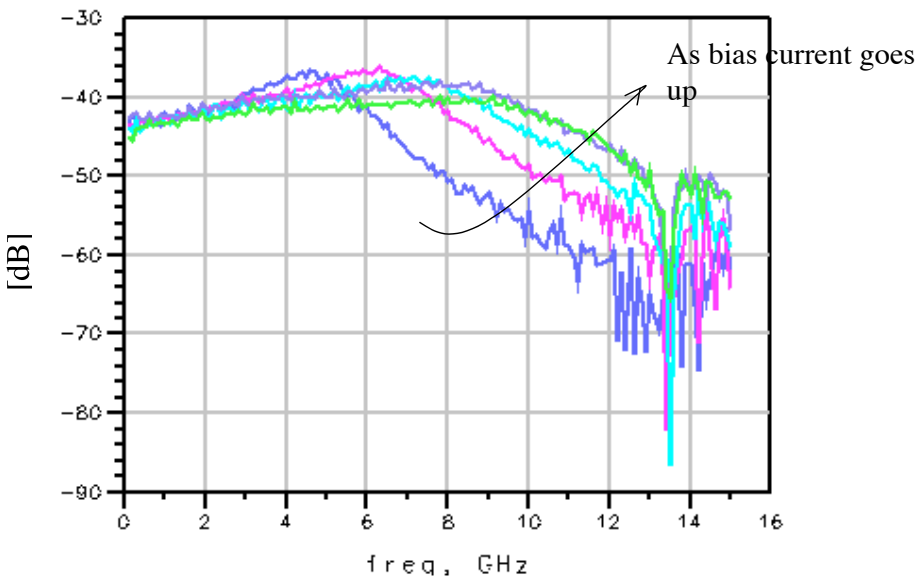


Figure 2.15. Forward transmission characteristic of the VCSEL.

Figure 2.15 shows the forward transmission characteristic of the VCSEL. The bias current is from 2 mA to 6 mA by 1 mA step size. Resonant frequency is increased as

the bias current goes up. The small-signal modulation bandwidth is up to 10 GHz with the bias current above 2 mA.

2.3.3 VCSEL MODEL DEVELOPMENT

The circuit-based VCSEL model is composed of two parts. First, the I-V relation with the small-signal input impedance characteristic is described by the electrical model part and second, the static L-I relation and forward transmission characteristic is described via a well-known rate equation. For the input impedance characteristic of the VCSEL, we used the diode equation with series resistance, which accounts for the differential resistance ($\frac{dV}{dI}$) of the VCSEL. Also, accounting for the parallel junction capacitance and series inductance, we successfully modeled the small-signal input impedance characteristic of the VCSEL. Figure 2.16 shows the circuit description for the electrical characteristic of the VCSEL. Nonlinear resistance R* in Figure 2.16 is described via a simple diode equation. The extracted circuit component parameter is shown in Table 2.1.

Table 2.1. Extracted circuit parameter used in electrical characteristic model.

L1	L2	R	C1	C2
0.05nH	0.29nH	16	28pF	22pF

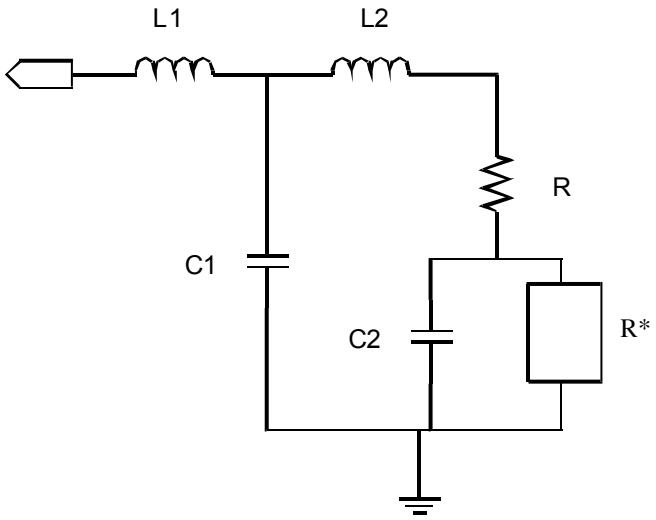


Figure 2.16. Circuit topology for electrical characteristic model.

Figure 2.17 shows the input impedance of the VCSEL model along with the measurement result. The VCSEL input impedance characteristic is successfully modeled at different bias conditions.

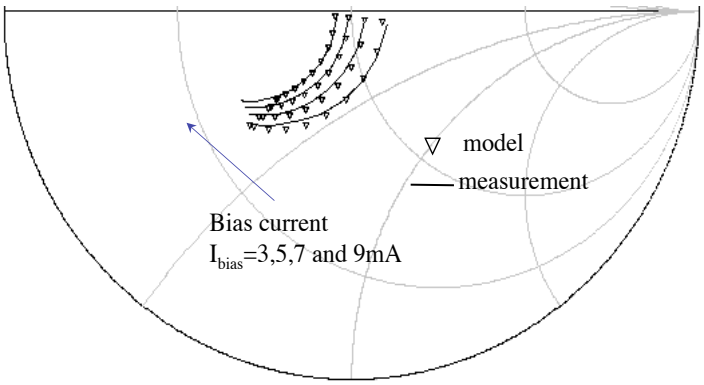


Figure 2.17. Input impedance characteristic of the VCSEL model with measurement result.

The offset current is introduced in the rate equation to account for the thermal effect on the L-I characteristic [21]. Different from the model developed in [21], the offset current (I_{off}) is derived as a function of the injection current (bias current). Via an empirical model of offset current, transient temperature differential equation is not required in this model. As a result, the modeling procedure is simplified. Equations (2.1) through (2.4) show the rate equation, which is modified by the introduction of the offset current.

$$\frac{dN}{dt} = \frac{\eta(I - I_{off}(I))}{q} - \frac{N}{\tau_n} - \frac{G_o(N - N_o)S}{1+\varepsilon S} \qquad (2.1)$$

$$\frac{dS}{dt} = -\frac{S}{\tau_p} + \frac{\beta N}{\tau_n} + \frac{G_o(N - N_o)S}{1+\varepsilon S} \qquad (2.2)$$

$$P_0 = kS = (v_s + \delta) \qquad (2.3)$$

$$N = Z_n v_n \qquad (2.4)$$

The offset current,

$$I_{off}(I) = a_0 I + a_2 I^2 + a_3 I^3 + a_4 I^4$$

is derived empirically from the differential slope efficiency η and measured L-I characteristic. In the rate equation, S is the photon number, N is carrier number, τ_n and τ_p are carrier recombination lifetime and photon lifetime respectively. β is spontaneous coupling coefficient, ε is gain compression factor, N_o is carrier transparency number, and G_o is the optical gain coefficient. Optical power is modeled via P_0, and the coupling loss via k. Additional arbitrary parameters Zn and δ are used for the single solution of the rate equation [22]. Table 2-2 shows the rate equation parameters used in this model.

Table 2.2. Rate equation parameter used in this model.

τ_n	τ_p	G_0	N_0	β	η_i	K	Z_n	δ	ε
$5\cdot10^{-9}$	2.28 $\cdot10^{-12}$	10.8 $\cdot10^{4}$	1.94 $\cdot10^{7}$	$1\cdot10^{-6}$	1.08	2.6 $\cdot10^{-8}$	$1\cdot10^{8}$	$5\cdot10^{-10}$	11 $\cdot10^{-7}$

The above differential equations (1), (2) are modified to implement with the circuit components as shown in Figure 2.18. Injection current I in Figure 2.18 is the current equivalent to the current flowing nonlinear resistance R* in Figure 2.16. The circuit component parameters derived from the rate equation are as follows:

$$R_n = \frac{\tau_n \eta_i}{Z_n}\ ,\ C_n = \frac{Z_n q}{\eta_i}, \text{ and}$$

$$I_n = \frac{G_o q (Z_n v_n - N_o)(v_s + \delta)^2}{k\eta_i (1 + \varepsilon \frac{(v_s + \delta)^2}{k})}$$

which compose the circuit in Figure 2.18 (a), and

$$R_s = 1,\ \ I_s = \frac{\beta Z_n v_n \tau_p k}{\tau_n (v_s + \delta)},\ \ C_s = 2\tau_p, \text{ and}$$

$$I_{ss} = \frac{G_o (Z_n v_n - N_o)(v_s + \delta)\tau_p}{1 + \varepsilon \frac{(v_s + \delta)^2}{k}} - \delta$$

which is implemented via the circuit in Figure 2.18 (b).

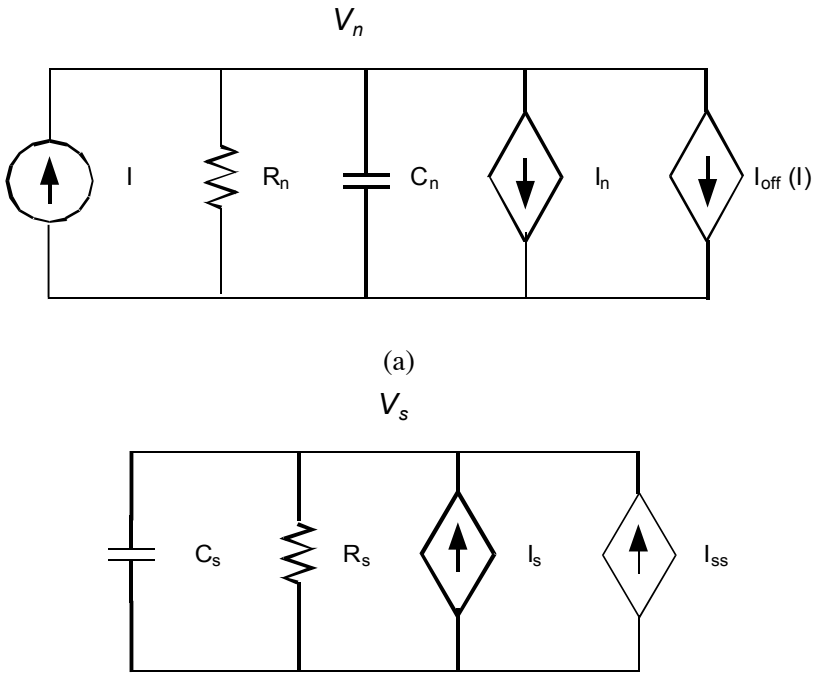


Figure 2.18. Equivalent circuit model to modified rate equation. (a) Equivalent circuit to equation (1). (b) Equivalent circuit to equation (2)

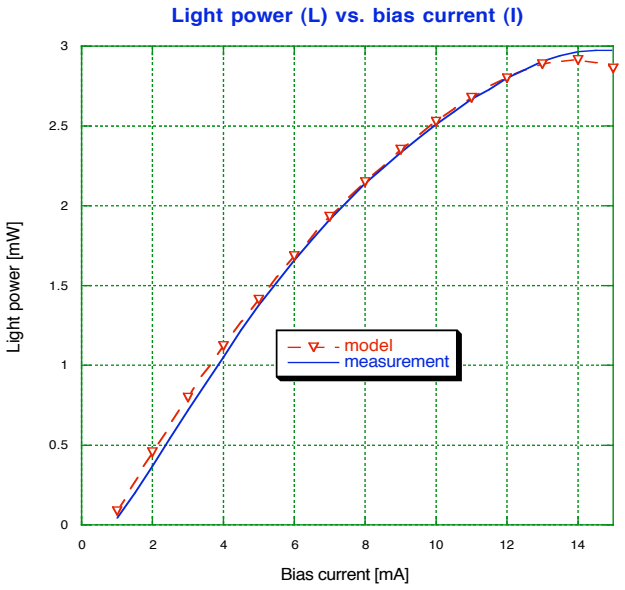


Figure 2.19. Nonlinear L-I characteristic measurement and model performance.

Figure 2.19 shows the measured L-I characteristic and model performance. The thermal roll-over is successfully modeled by introducing the empirically modeled offset current.

The rate equation enables the description of the small-signal forward transmission characteristic of the VCSEL as well. Figure 2.20 shows the measured forward transmission characteristic and model performance. With various bias point such as 2,3,4, and 5mA, the rate equation-based VCSEL model matches well with the measurement result. At the same time, the nonlinear L-I characteristic models the VCSEL nonlinear effect, such as harmonics and mixing effect.

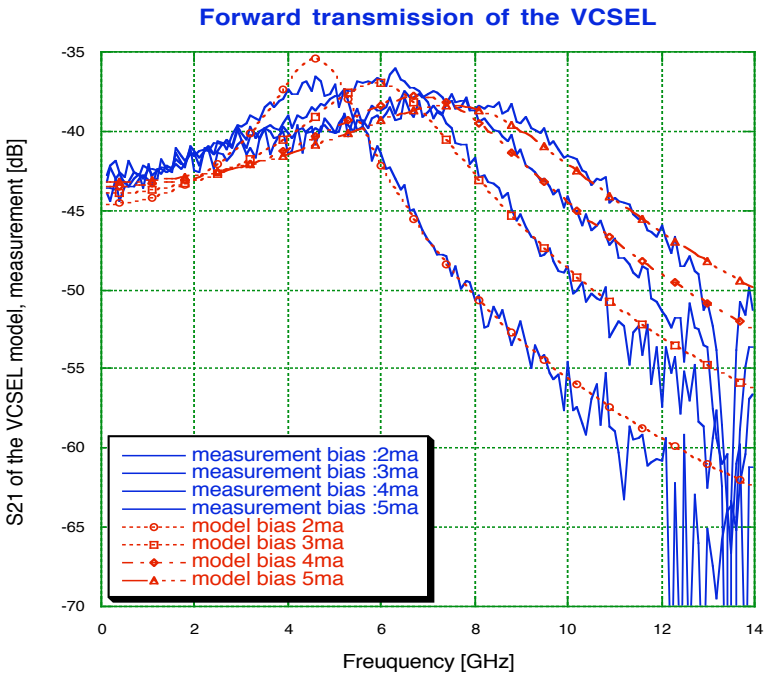


Figure 2.20. Forward transmission characteristic and model performance (bias current: 2,3,4, and 5mA).

2.4 OVERALL OPTICAL LINK EXPERIMENTAL RESULT

The combined digital/wireless link is simulated via the circuit-based VCSEL model, which was developed in Section 2.3, and the transmission line-based combiner model. Overall simulation is performed in the transient response engine and the spectrum is taken from the time domain data. Figure 2.21 shows the overall link simulation setup in the transient response simulation engine. The link simulation result is shown in Figure 2.22. The eye diagram is taken after coupling out the RF spectrum, and the overall link spectrum is taken at the output port of VCSEL model.

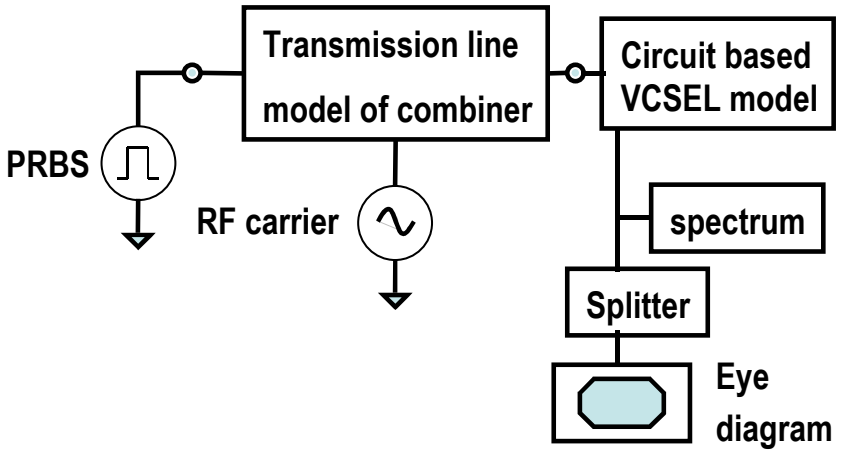


Figure 2.21. Hybrid link simulation block diagram.

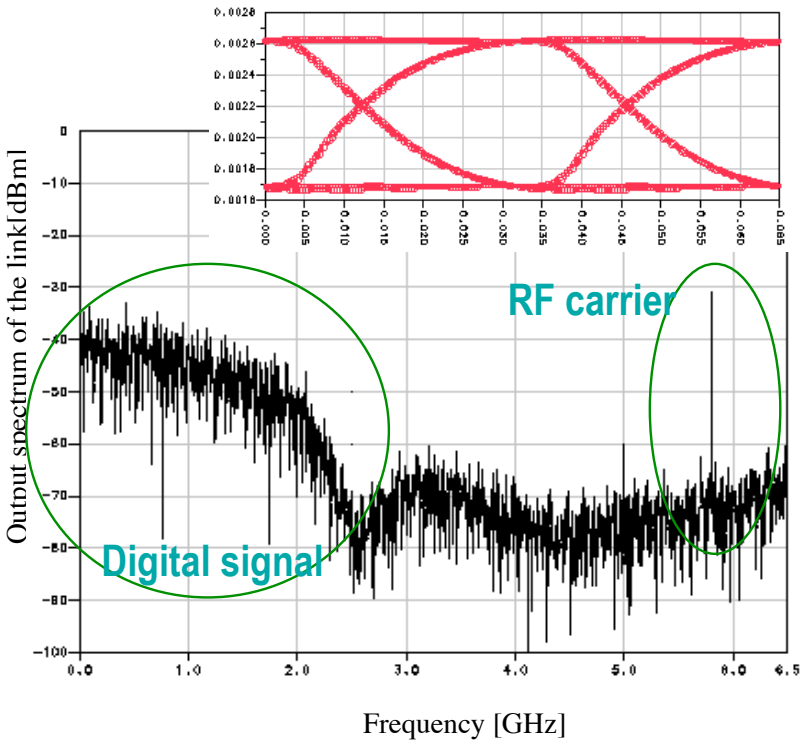


Figure 2.22. Simulation result of the overall link spectrum and the eye diagram of the baseband signal via VCSEL and combiner model.

For the overall link measurement, an OC-48 data stream and an 802.11a WLAN signal are incorporated and applied to the combined link transmitter. The WLAN signal is generated from the HP-4438 signal generator. For the optical link characterization purposes, an 802.11b WLAN signal is also generated with a carrier frequency at 5.8 GHz. A 100 m MMF with a 50 μm core size is directly coupled to the VCSEL. The combined signal is detected at the photo-receiver and is fed through the combiner again on the receiver side. In the receiver side, the combiner works as splitter. The entire link spectrum is shown in Figure 2.23. When the two signals are transmitted simultaneously, the baseband data signal is mixed with the wireless signal because of the nonlinear L-I characteristic of the VCSEL. As a result, there is a small

amount of frequency regrowth on the RF spectrum, as shown in Figure 2.23. However, by adjusting the bias current of the VCSEL and the baseband signal power level, the frequency regrowth can be minimized, as shown in Figure 2.24. Figure 2.25 shows the detailed spectrum of the received WLAN signal.

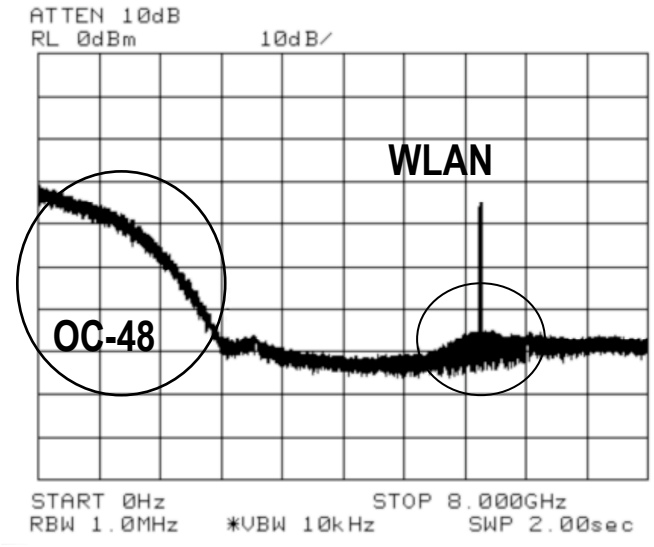


Figure 2.23. Overall spectrum with spectrum regrowth at RF side.

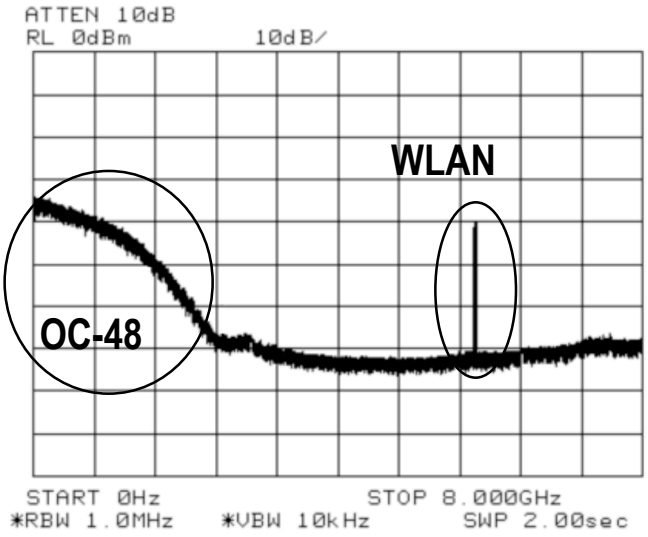
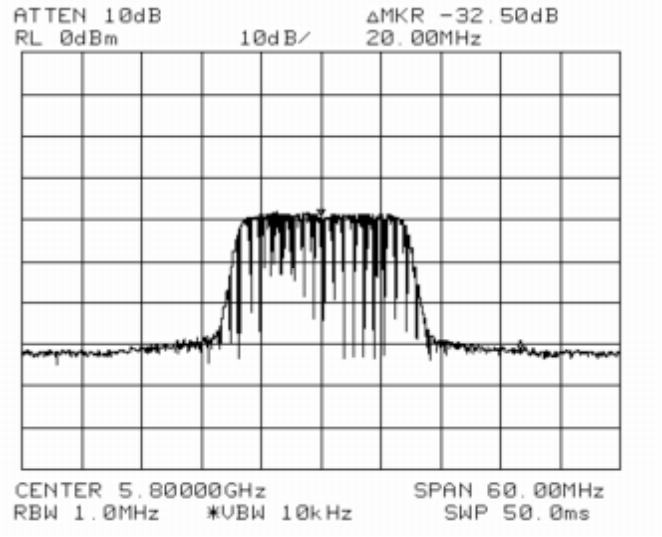
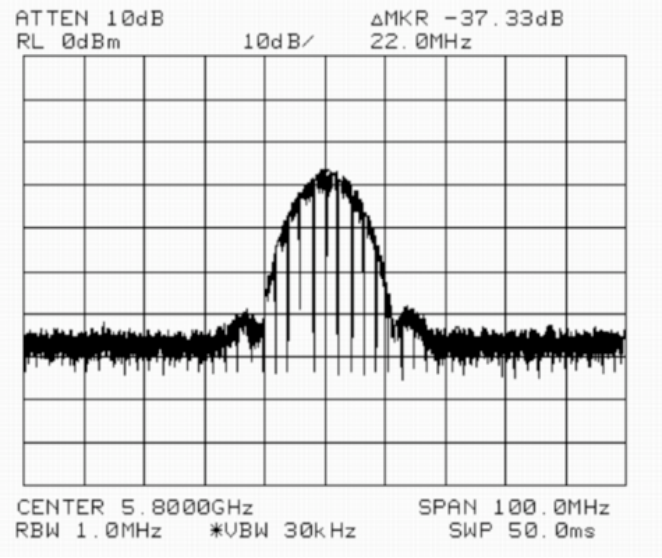


Figure 2.24. Overall spectrum of the received signal by adjusting the VCSEL bias current and baseband signal power level.



(a)

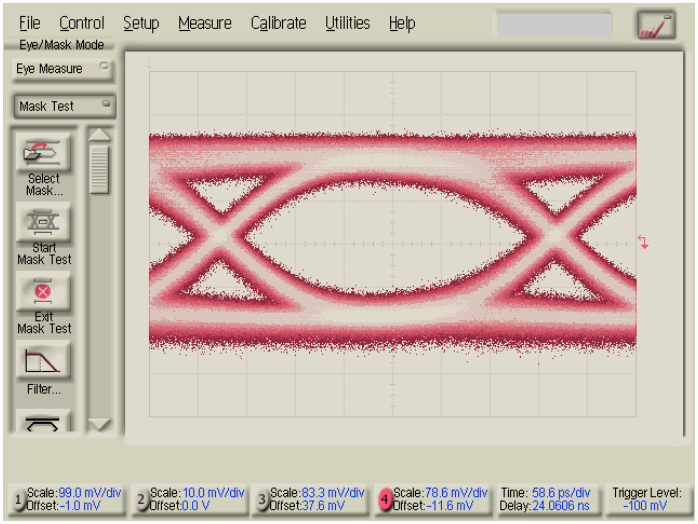


(b)

Figure 2.25. WLAN spectrum at the receiver side. (a) 802.11a WLAN signal at 5.8Ghz. (b) 802.11b WLAN signal at 5.8Ghz.

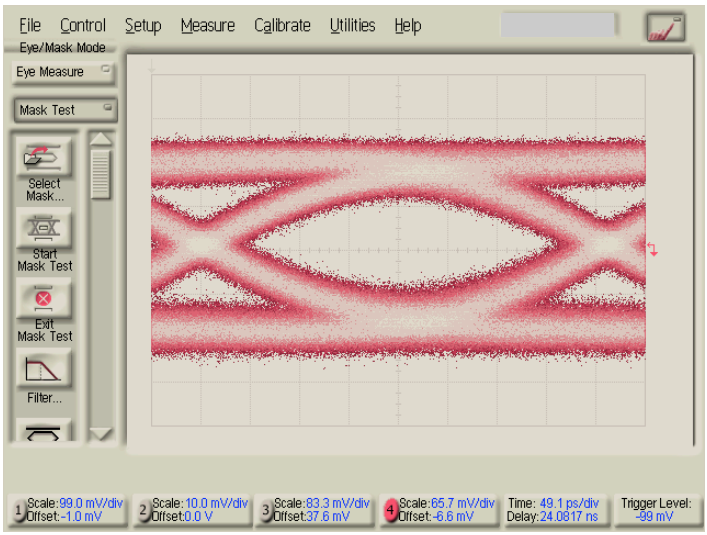
The eye diagram of the baseband signal is shown in Figure 2.26. The modal dispersion of the MMF shrinks the eye opening of the received signal. The modal dispersion is

characterized by the bandwidth-distance products. The currently available MMF has a 160 MHz·km bandwidth distance product for 850 um wavelength and 500 MHz·km for 1300 um. However, recent research has shown that the passband beyond the modal dispersion bandwidth of the MMF is usable for transmission of additional data [23]. In this system, the wireless signal at 5.8 GHz is successfully transmitted beyond the modal dispersion bandwidth of the MMF via the passband region of the MMF. Finally, Figure 2.27 shows the implemented hybrid optical link over the multi-layer organic board.



(a)

Figure 2.26. Eye diagram of the baseband signal. (a) Baseband signal (OC-48) before 100m MMF. (b) Baseband signal (OC-48) after 100 m MMF



(b)

Figure 2.26. Continued

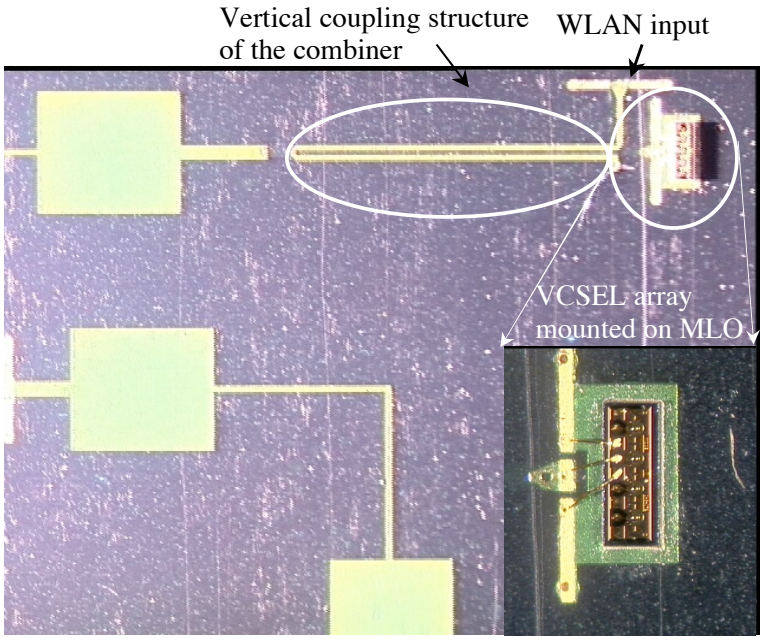


Figure 2.27. Picture of the hybrid optical link.

So far, the combined digital/wireless link with VCSEL is described with some technical detail such as the combiner design, VCSEL modeling, experimental result for

the optical link using MMF. In the following chapter, the equalization to increase the usable distance of the MMF will be covered. By this way, the distance of the MMF for combined link can be increased further.

CHAPTER III

EQUALIZATION TO COMPENSATE FIBER DISPERSION

In this chapter, the equalization to compensate the dispersion in fibers is described. Section 3.1 briefs the different fiber types with their characteristics and applications. Also the three major types of dispersion in fibers are described including the cause and effect of three different dispersions respectively. Section 3.2 covers brief history of the efforts to compensate the fiber dispersion mainly through the optical and electrical approaches. In the following section, the various types of equalizers are covered from a system and an implementation point of views. The equalizer is mainly classified as a linear equalizer, a nonlinear equalizer, an adaptive equalizer, and a bode-type equalizer. The transmitter side equalizer and the receiver side equalizer are covered with their pros and cons regarding the practical implementation issues.

3.1 DISPERSION IN FIBERS

It is necessary to review the different types of fibers with their characteristics before covering the fiber dispersion, because the dispersion in the fibers depends on the fiber types. In this dissertation, three major types of fibers are reviewed as follow:

1) step-index MMF, 2) graded-index MMF, and 3) single mode fiber (SMF).

MMF has been used mainly with the light sources such as light emitting diode (LED) for short-haul application. A large core diameter of the MMF has the merit of collecting light efficiently from inexpensive light sources. However, MMFs can generate multi-modes of light lay in the fiber, which is undesirable effect from a communication perspective. Multi-mode generation depends on the core diameter, a numerical aperture, and light launch conditions.

As multi-mode properties introduce modal dispersion, which limits the MMF usage in optical communication, a fiber with a gradual refractive index profile is developed (graded-index MMF). The faster light speed in the low refractive index compensates the differential modal delay effects, which are severe in the step-index MMF. The MMFs with core sizes of 50 um and 62.5 um are standard for short-distance fiber communication. The main application of the multi-mode fibers today is in systems where connections must be made inexpensively, and transmission distances and data speeds are modest. However, the MMF still is not ideal candidates for long-haul optical communication.

The SMF has a small core size, which is small enough to restrict transmission to a single mode. Because the single-mode transmission avoids modal dispersion, modal noise, and all other effects that come with multi-mode transmission, SMFs can carry signals at much higher speeds, and longer distances than MMFs. As a result, the SMF is used widely over long-haul fiber-optic communication systems. Figure 3.1 shows the core size of the fibers and conceptually describes how the light is transmitting over the MMFs and SMFs.

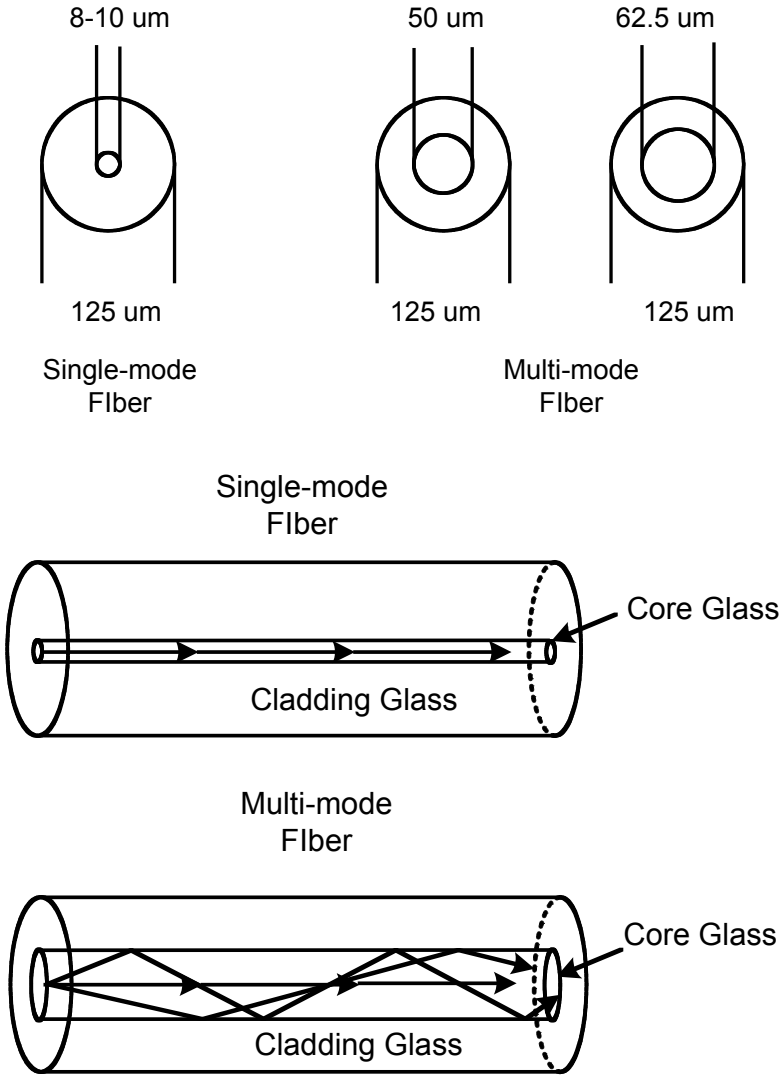


Figure 3.1. Light transmission over SMF and MMF.

The major concerns in fiber communication are the dispersion, which generates ISI and becomes severe as the data speed and distance are increased. In this dissertation, three different types of dispersions are briefly reviewed. First, DMD is the dispersion as the numerous guided modes are transmitted with different paths in the MMF resulting in different receiving time at the receiver side of the fiber communication system. The

DMD becomes a severe factor as the length of the MMF is extended or the data rates are increased. By these reasons, the MMF is specified by the bandwidth-distance product. Figure 3.2 shows the ISI penalty versus distance plot in different bandwidth-distance product MMFs assuming 10 Gbps data throughput. Because of the DMD, MMF usage is limited to short-haul applications.

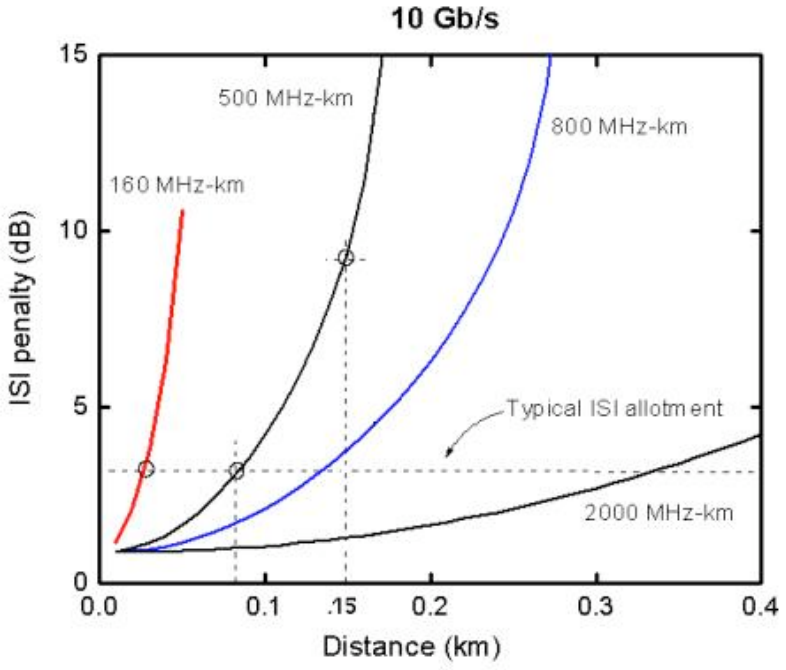
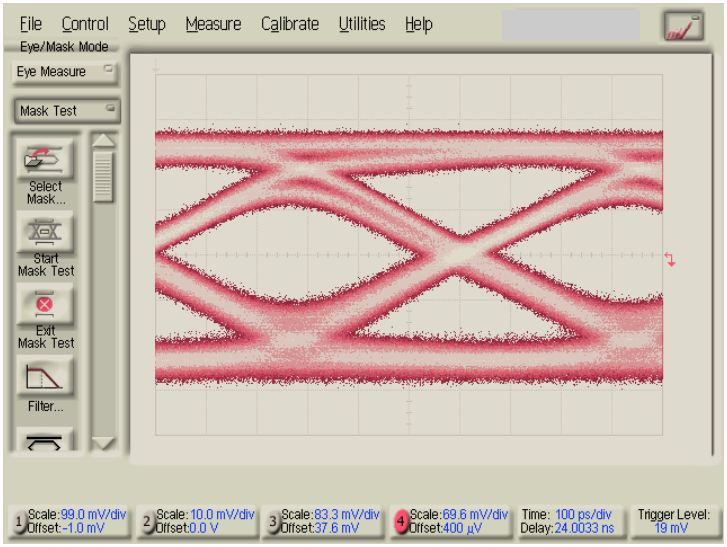


Figure 3.2. ISI vs. distance plot with different bandwidth-distance product [24].

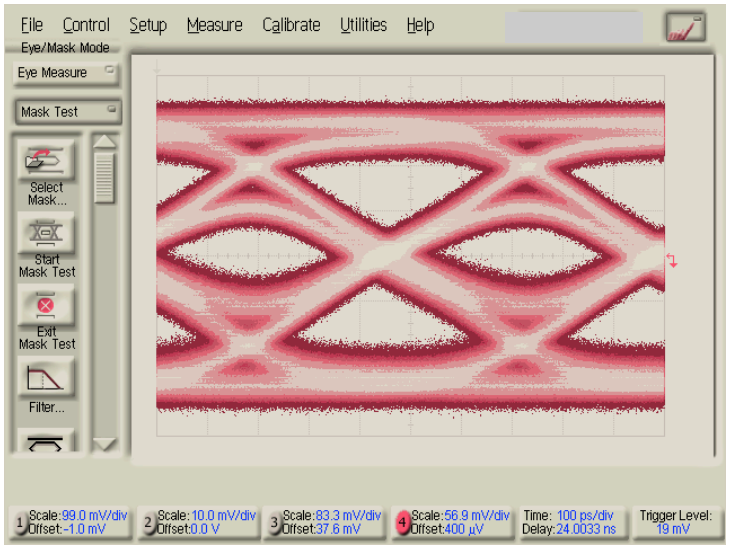
Second is polarization-mode dispersion (PMD), which is generated when the two polarization modes in the SMF experience slightly different conditions and travel along the fibers at different speeds as a result of the generic imperfect circular symmetry of the fibers and other external stress on the fibers. Finally, the chromatic dispersion (CD) is caused by the variation in the speed of light through the fiber depending on a wavelength.

The CD is the sum of two quantities, dispersion inherent to the material and dispersion arising from the structure of the waveguide. With the PMD, the CD is the main dispersion factors in a SMF. However, for the MMF, DMD is the main dispersion factors and PMD and CD can be neglected. Figure 3.3 shows the eye diagram of the received signal from a photoreceiver through the MMF with VCSEL as light sources. As the data rate increases, the eye diagram experiences more dispersion resulting in increased ISI penalties.



(a)

Figure 3.3. Eye diagram dispersion due to DMD in MMF. (a) 1.5Gbps PRBS after 300 m MMF. (b) 1.85 Gbps PRBS after 300 m MMF.



(b)

Figure 3.3. Continued.

3.2 HISTORICAL BACKGROUND TO COMPENSATE DISPERSION IN FIBER

To compensate fiber dispersion, several methods are researched and reported. For the CD compensation in SMFs, a dispersion-compensating fiber is inserted at the end of the installed optical path. As the dispersion-compensating fiber has an opposite dispersion direction from the installed fiber, the overall dispersion can be compensated at the optical receiver front end. Typically, the compensating fiber fabricated via fiber grating has several times higher magnitude in the dispersion, requiring a shorter length of dispersion-compensating fiber [25]. The PMD can be compensated via birefringence. Since the PMD can be regarded as an optical-birefringence fluctuation with time and wavelength, the most straightforward approach is to insert adaptively tuned birefringence, opposite to the link PMD, into the optical path at the receiver input port [26]. The DMD reduction is achievable if only a subset of the fiber mode can be excited on a fiber [27]. This was achieved by launching the light from a SMF into the center of the MMF, which resulted in a small number of low-order modes being excited [28]. Also, offset launching to the MMF reduces the number of excited modes, resulting in an increased bandwidth-distance product in MMF [29]. Different from pure optical domain approaches, optoelectronic type of the DMD compensation methods are reported [30]. The spatial diversity of the emitted signal at the output of the MMF is exploited with a multisegment photodetector. The use of multisegment photodetector in [30] is analogous to the use of multiple antennas in wireless communication to compensate the multipath-fading effects.

Most of the dispersion-compensation researches have thus far appeared in the optical domain; however, it is still expensive and bulky solutions. Therefore, it is desirable to exploit the vast pool of signal processing knowledge to suppress the ISI in electrical domain. Electronic equalizations already have been used in a copper channel, where compensation of echoes, frequency dependent loss characteristics, and the interference from adjacent channels has enabled the dramatic transmission data rate improvements of telephone modems and digital subscriber line (DSL) connections. By further extending these algorithms and implementing them with the latest high-speed analog and mixed signal circuit techniques, significant compensation for many of the impairments observed in fiber can be achieved.

For example, a linear equalization (transversal filter), a nonlinear equalization, and a maximum likelihood detection technique are studied to reduce the PMD, the light source nonlinearity, and the CD in fiber optic networks [31, 32, 33]. Winters *et al*. show the initial feasibility of electrical signal processing to compensate the optical system channel induced impairments [31]. Also, the PMD and CD mitigation was presented previously by concatenation of a decision feedback equalizer (DFE) and a FFE in a board-level implementation with the least mean square (LMS) algorithm [34]. The DMD compensation in electrical domain is also presented in [35]. With a 1300 nm wavelength light source, Zhao *et al*. presented 10 Gbps data transmission over a 1.5-km-long MMF. The overall equalizer is implemented on a board level and it still need to be implemented on a single IC. The DFE is selected as the equalizer architecture with the LMS algorithm. The author assumed three major modes in MMF and used two taps to compensate the two lower modes. Recently, high-speed SiGe-based FFE was reported [36]. To address the

high-speed operation problem in equalizer IC, distributed circuit technique has been adopted in the FFE. Distributed circuits are good candidates for high speed circuit operation because of their intrinsic wideband characteristics, which is originally come from the traveling wave amplifier (TWA) [37]. *Wu et al*. implement distribution network by LC ladder type of artificial transmission line, which supports continuous time signal delay for transversal filter type equalizer. All seven taps with tap coefficient multipliers are used to compensate the DMD for 10 Gbps NRZ data transmission over 800 m MMF. The authors used the 850 nm VCSEL as the light source and a 50 um core size of a next-generation MMF as a fiber channel.

In this dissertation, the DMD compensation using an FFE is described [38, 39]. Two different types of the FFE are implemented as an IC via standard 0.18um CMOS process. One used the artificial transmission line for a continuous time tap delay elements. The current summation node is directly connected to the output of the equalizer by optimizing the parasitic effects differentiating it from [36] in overall circuit configuration. The other type of the FFE is implemented with active circuit components as the continuous time tap delay elements. The detailed explanation regarding the developed FFEs is described on the chapter 4 and 5.

3.3 EQUALIZER TOPOLOGY STUDY

The basic function of the equalizer is to compensate any signal distortions or any general losses resulting from the channel loss characteristics. The simple linear equalizer has the equivalent mathematical transfer function as follow:

$$G_E(f) = \frac{1}{C(f)} = \frac{1}{|C(f)|} e^{-j\theta_c(f)} \qquad (3.1)$$

where, *C(f)* is the channel characteristics and $G_E(f)$ is equalizer transfer function characteristics [40]. Therefore the amplitude response of the equalizer is $|G_E(f)| = 1/|C(f)|$ and its phase response is $\theta_E(f) = -\theta_c(f)$. As the equalizer transfer function is inverse form of the channel, the equalizer completely eliminates the ISI cause by channel. This equalizer is called zero-forcing equalizer.

For example, the copper channel such as telephone line or twist cable, has low pass filter characteristics resulting in increased rising time and falling time of the transmitted signal. The increased rising time and falling time causes the ISI, in other words, the dispersion in the channel impulse response. The ISI is the main source of the signal distortion in digital communication systems. Figure 3.4 shows the conceptual view of the signal dispersion in lossy channel.

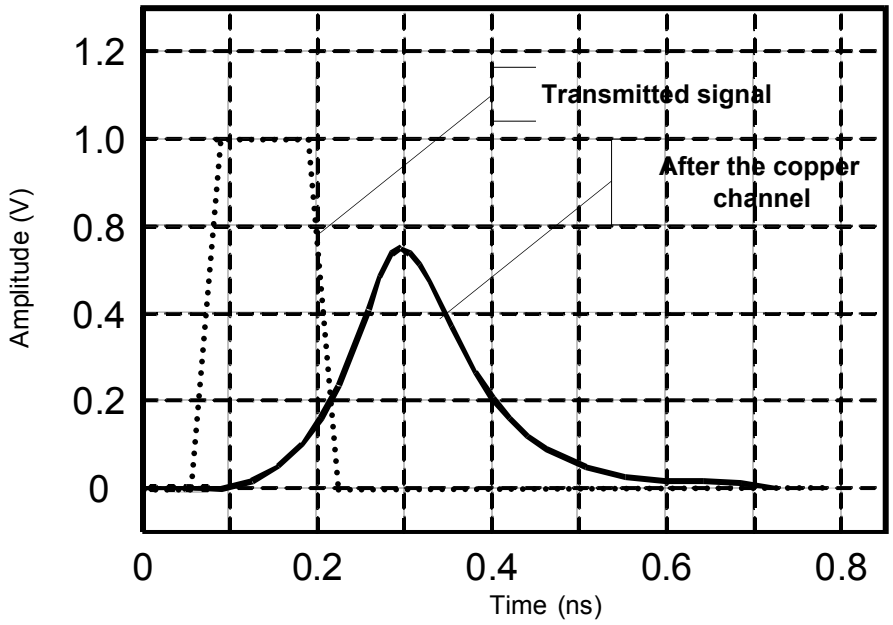


Figure 3.4. Channel impulse response dispersion in copper channel.

Through the equalization at the receiver side, one can rebuild the transmitted signal shape from the dispersive signal at the receiver front end. This work can be done in the receiver side as explained above, or the signal can be transmitted with some intended signal distortion at the transmitter side. This is called pre-emphasis technique. This section will touch the background knowledge of equalization, various types of equalizations, and the pros and cons of the each equalization techniques.

3.3.1 LINEAR EQUALIZER

Most common types of a channel equalizer used in practice to compensate ISI are a linear FIR filter with adjustable tap coefficients as shown in Figure 3.5. Each tap coefficients are updated through the certain equalization algorithms. With the FIR structure implementation, there are several equalization algorithm criteria to reduce the ISI.

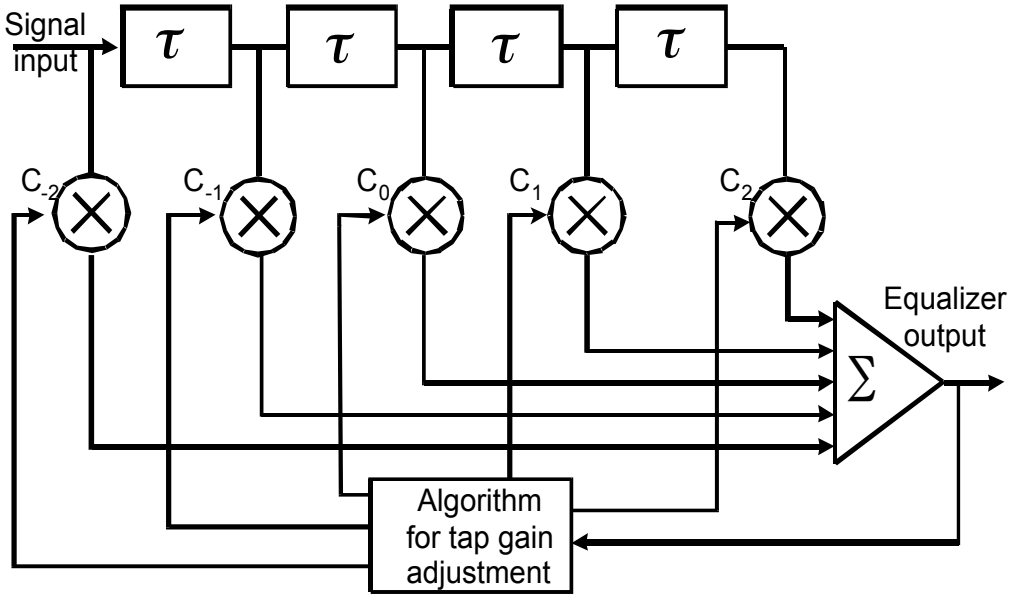


Figure 3.5. Linear FIR equalizer.

Most simple linear equalizer type is the zero-forcing equalizer as described previously. The zero-forcing equalizer has the transfer function characteristics as described in equation 3.1. The time delay element in Figure 3.5 is called tap delay. The tap delay can be as large as symbol interval so the delayed version of the signal is $x(t-k\tau)$ (where

τ=T, T is the symbol period of the signal, and k=1, . . . , n). Also τ can be smaller than T, in this case, it is called fractionally spaced equalizer. The fractionally spaced equalizer can reduce the aliasing problem in a symbol spaced equalizer and improve the performance assuming the delay is implemented by sampling [41]. As the zero forcing equalizer has inverse channel transfer function characteristics, it can significantly increase the additive noise in the channel. An alternative solution to ameliorate this problem is the minimum-mean-square-error (MMSE) algorithm, where the tap value is optimized to minimize the power in the residual ISI and the additive noise in the channel.

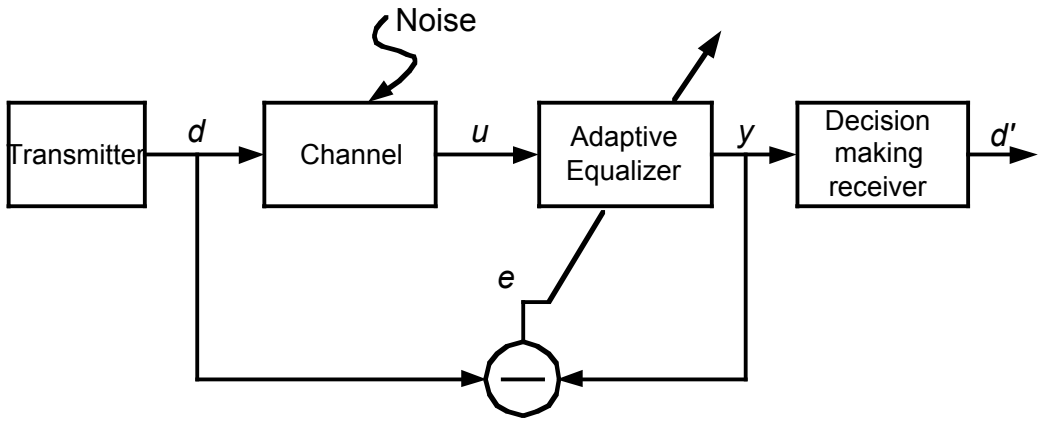
If the channel frequency dependent loss characteristics are time-invariant, the channel can be measured and the tap coefficients for the equalization can be extracted from the measured channel characteristics. As the channel is time-invariant, once the tap coefficients are set, the data can be transmitted without further adjusting the tap values. However, if the channel is time-variant such as the wireless channel, the equalizer tap values should be updated periodically based on the real-time channel frequency characteristics. The equalizer that can update the tap value by tacking the channel characteristics is called adaptive equalizer. Most commonly used adaptive equalization algorithm is LMS algorithm [42]. The tap coefficients to be updated based on the LMS algorithm are shown as follow:

$$p(k+1)=p(k)-\mu\frac{\partial E[e^2]}{\partial p} \ or$$

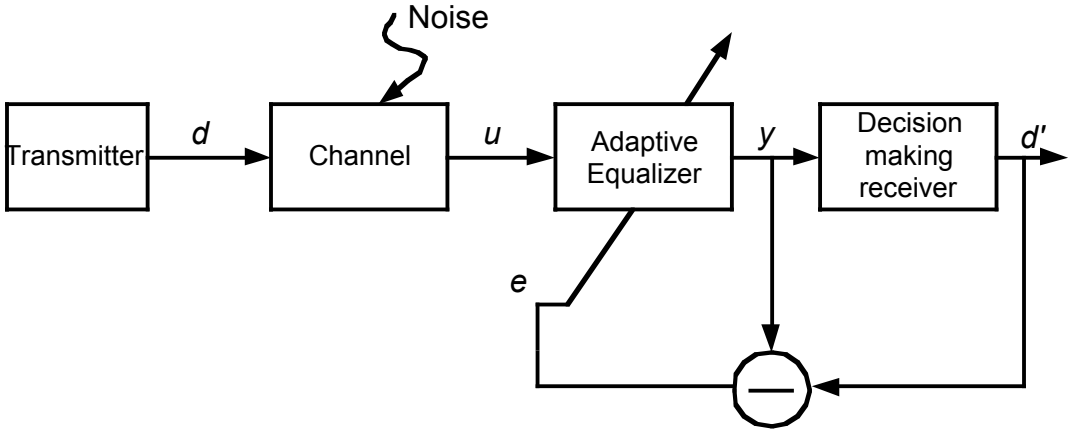
$$p(k+1)=p(k)+2\mu\cdot e(k)\cdot\phi(k) \qquad (3.2)$$

where p(k) is the tap coefficients, μ is the parameter controlling the adaptation rate, $e(k)$ is the error signal between the desired signal and received signal, and ϕ(k) is the

derivative form of the received signal (i.e. $\frac{\partial y}{\partial p}$, where y is the signal after the adaptive equalization). Figure 3.6 shows the one example of adaptive equalization. In this example, the transmitted signal is required at the receiver side (i.e. training sequence) as shown in Figure 3.6 (a), or desired signal can be extracted from the receiver's decision block as shown in Figure 3.6 (b).



(a)



(b)

Figure 3.6. Adaptive equalization (a) using training sequence and (b) using the decision signal at the receiver as the desired signal.

The practical implementation of the LMS algorithm still requires lots of hardware. So there are several alternative simplified algorithms to reduce the burden in hardware implementation. The simplified version of LMS algorithms is as follow [43]:

Sign-data LMS: $p(k+1)=p(k)+2\mu \cdot e(k) \cdot sgn(\phi(k))$

Sign-error LMS: $p(k+1)=p(k)+2\mu \cdot sgn(e(k)) \cdot \phi(k)$

Sign-sign LMS: $p(k+1)=p(k)+2\mu \cdot sgn(e(k)) \cdot sgn(\phi(k))$

Eventhough the advantage in hardware implementation, these simplified algorithms have potential that they may not converge and they may have slower adaptation time than the original algorithm.

3.3.2 NONLINEAR EQUALIZERS

Linear equalizers described in previous section are very effective on channels, such as wire line telephone channels, where the ISI is not severe. However in some channel environments, for example the channel where spectrum null exists, the linear equalizer will introduce large amount of gain to compensate the spectrum null. Thus the noise in the channel will be enhanced severely. Such channels are often encountered in mobile radio channel, such as those used for cellular radio communications.

A DFE is a nonlinear equalizer that employs previous decisions to eliminate the ISI caused by previously detected symbols on the current symbol to be detected. The block diagram for the conventional DFE is shown in Figure 3.7.

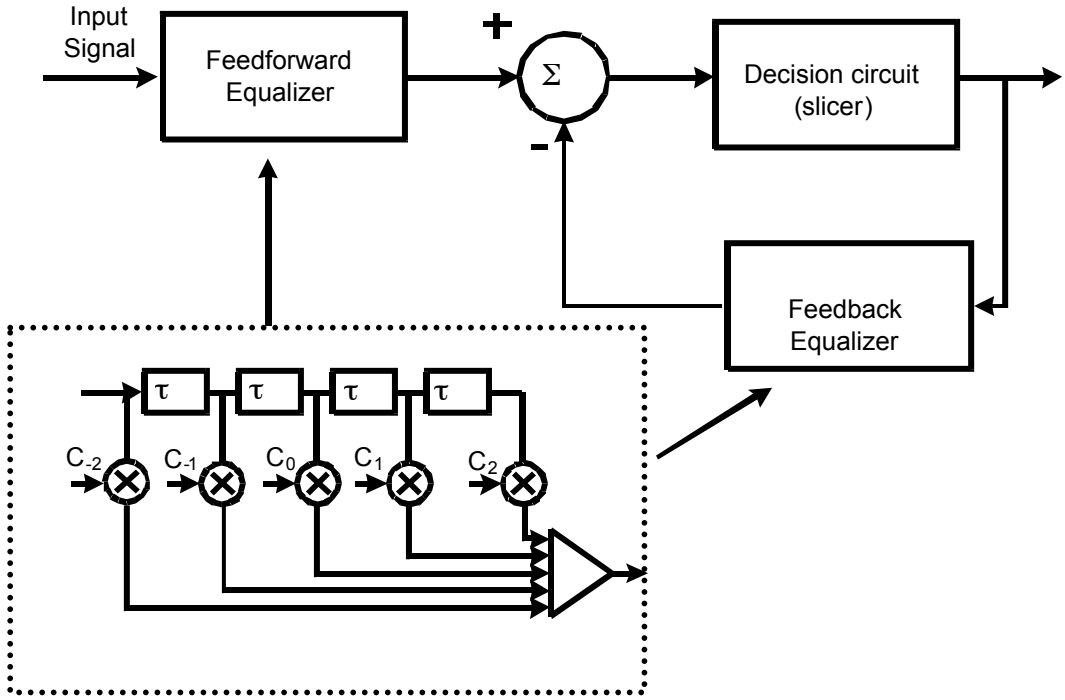


Figure 3.7. Block diagram of the conventional DFE.

The DFE is typically used with the conjunction of linear FFE as shown in Figure 3.7. Eventhough the linear FFE alone can be used to cancel the ISI, the combination of the linear FFE and DFE has better performance. The principle reason for this improvement is that the DFE uses the linear combination of the noiseless binary decisions to eliminate some of the ISI and does not add noise at the input of the decision circuit. The linear FFE amplifies the high-frequency portion of the signal and the noise to cancel the ISI, which is not compensated by DFE. So the noise enhancement of the linear FFE in conjunction with DFE is less than the one when the linear FFE alone is used. Recently, the DFE is reported as a good candidate for backplane channel equalization, where the near-end-crosstalk is severe [44]. Otherwise the FFE alone will significantly amplifies the near-end-crosstalk because the near-end-crosstalk frequency response is similar to the high

pass filter response. One potential problem with a DFE is the error propagation [43]. If the DFE outputs an incorrect decision, the error will propagate through the feedback filter and increase the probability that another incorrect decision will be made.

There is another algorithm, which finds the sequence that maximizes the joint probability of the received sequence conditioned on desired sequence. This sequence is called the maximum-likelihood sequence detector. An algorithm that implements maximum-likelihood sequence detection (MLSD) is the Viterbi algorithm. Partial-response maximum-likelihood (PRML) detectors using various implementations of the Viterbi algorithms are a popular choice for hard disk drive read channel, where digital communication techniques are adapted to combat the ISI [45, 46]. The major drawback of MLSD is the exponential behavior of the computational complexity, which is a function of the ISI span. Thus the MLSD is practical for the channel where the ISI spans only a few symbols [40].

3.3.3 CABLE EQUALIZER (BODE EQUALIZER)

In this section, one typical form of the equalizer specifically for the cable channel will be covered. As the cable channel can be modeled with simple low pass filter transfer function, the cable equalizer can be implemented with the combination of the high pass filter with several poles as design parameters and variable gain controller as shown in Figure 3.8.

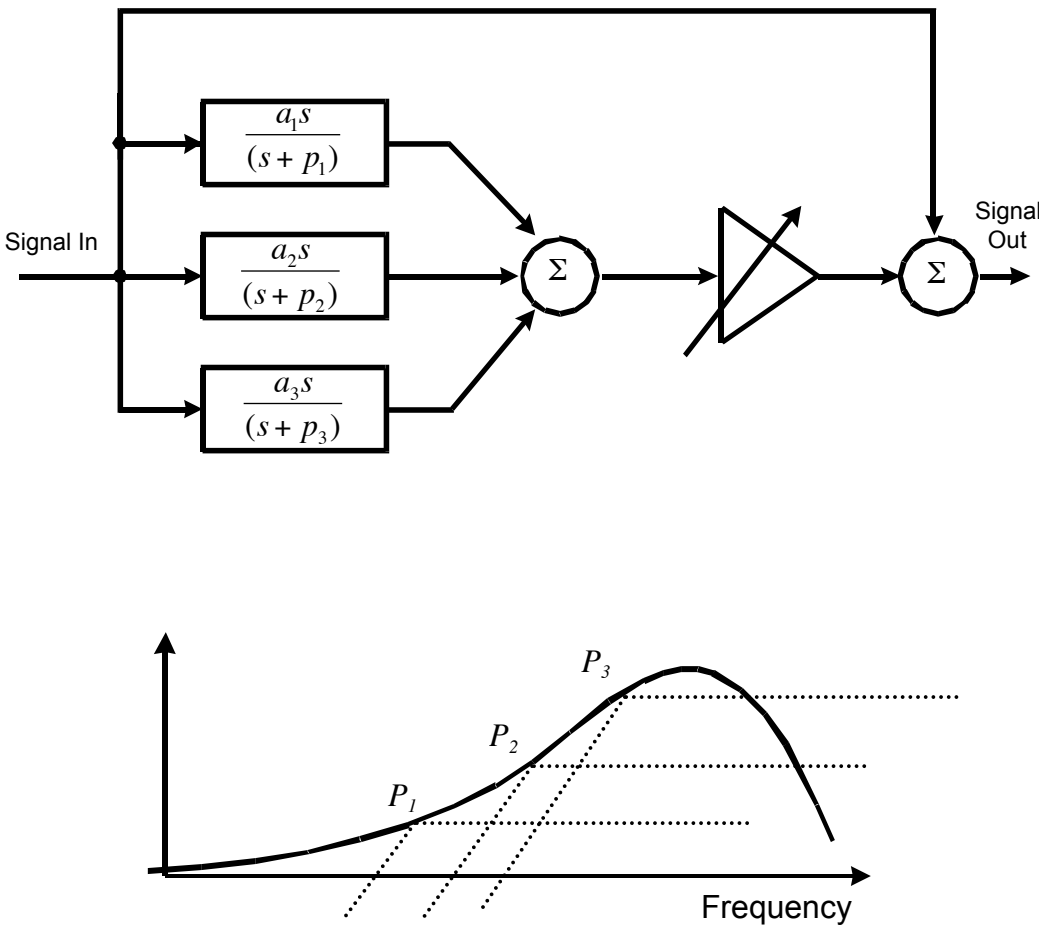


Figure 3.8. Block diagram for the simple cable equalizer.

The variable gain can be controlled via a LMS or other algorithm for adaptation. The cable equalizer is practical to implement by analog continuous time signal processing compared to other type of equalizer. The continuous time equalization techniques have some advantage over discrete time counterpart. For example, the continuous time equalizer does not need any sampling phase recovery block, so that the equalizer adaptation can be realized independently with the timing recovery function [47]. Also the continuous time equalization is well fit for high-speed operation over the discrete time counterpart as it does not need any high-speed sampling function. Eventhough these

advantages, the cable equalizer has some potential problem that it can boost up the high-frequency noise, which is analogous phenomenon in the linear FFE.

3.3.4 TRANSMITTER AND RECEIVER SIDE EQUALIZER

As it is mentioned previously, the equalizer can be installed at the transmitter side or receiver side. The conceptual block diagram is shown in Figure 3.9. The transmitter side equalizer, which is called pre-emphasis has an advantage over receiver side equalizer such as ease to build by FIR filter type with digital control. However, firstly, the pre-emphasis boost up the high-frequency portion on the transmitter side so that it can increase the near-end-crosstalk for high-speed chip-to-chip interconnections. Secondly, the pre-emphasis requires the information sent from the receiver side for dynamic or fine-tuned tap coefficients updates. Finally, as channel loss increases, the pre-emphasis needs to apply more gain to boost the high frequency components of the transmit signal. Since the maximum signal swing is limited by the system constraints and the IC process technology, the average signal swing level at the transmitter side needs to be decreased thereby requiring additional gain at the receiver side. By these reasons, the equalizer at the receiver side is better candidate over the pre-emphasis for adaptive or fine tuned equalization. However as it is mentioned previously, the FIR type equalizer alone at the receiver side enhance the noise at high frequency ranges, while it compensates the channel loss to reduce the ISI. This is the one of the reason why we use DFE with combination of FFE, not just using FFE at the receiver side in the channel environment where the large amount of gain is required to compensate any severe spectral loss.

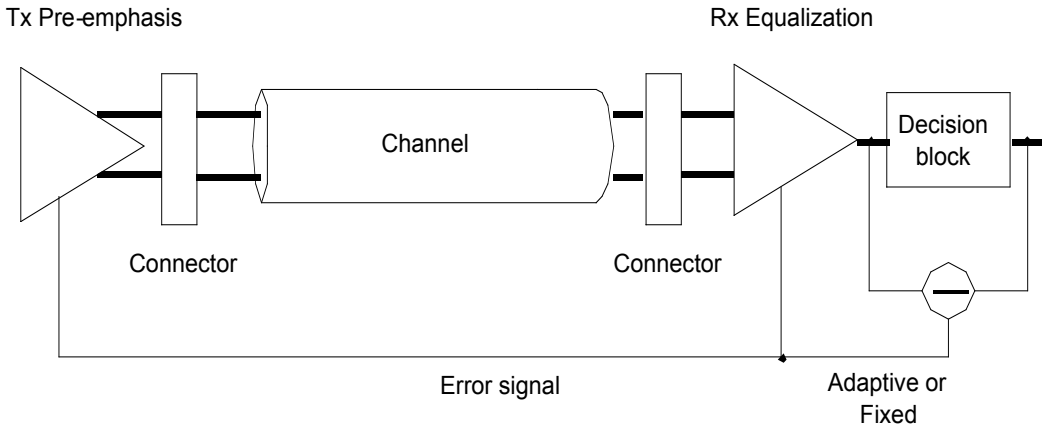


Figure 3.9. Equalization at the transmitter side, receiver side and both side.

It is also possible to use the combination of the pre-emphasis and receiver side equalization to further increase the overall bit error rate (BER) of the high-speed interconnections. By using the pre-emphasis and receiver side equalization simultaneously, the gain-boosting requirement for specific spectral loss can be relaxed for each equalizer. However it needs more complex hardware implementation increasing the overall system cost.

For the digital communication systems, the typical equalizer is implemented with digital circuitry as the required data rate is below Gbps. For example, the wireless communication system requires the equalization to compensate the multi-path-fading effects. The equalizer IC for this type of channel has been implemented by conventional digital circuitry because the required data rate is still far below 1 Gbps.

However, as the data rate is increased over multi-Gbps, the conventional digital approaches are not proper solution anymore. By this reason, several standard task forces have been made such as XAUI, PCI-express, and UXPI to address any high-speed

interconnection problems in system and packaging level. Also in an IC implementation point of view, there have been several efforts for equalizer IC implementation by approaching in continuous time analog signal processing, mixed signal circuit, or RF/microwave techniques over conventional digital circuit approaches [36, 48, 49].

In this chapter, various types of equalizer and the background knowledge for the equalization are described with several categories. The next two chapters will cover the specific equalizer for a given MMF channel. The detailed design procedure, system level performance and measurement results for the fabricated equalizer IC will be described as well. Chapter 4 describes the continuous time equalizer with passive delay line approaches. The measurement result with 500 m MMF is shown. Chapter 5 covers the equalizer with all active components approaches.

CHAPTER IV

FFE WITH PASSIVE LC DELAY LINE

In this chapter, the FFE with passive LC delay line approaches for MMF will be discussed. As we investigated from the previous chapter, it is appropriate approach to use continuous time analog or microwave techniques to overcome any bandwidth limitation for a given CMOS technology. The equalizer discussed in this chapter is the continuous time linear FFE with the tap delay line composed of passive LC ladder structure to emulate the transmission line. The signal summation node for the FFE is implemented by current summation with passive load, which is directly connected to the output of the equalizer by optimizing the parasitic capacitance. This approach differentiates it from [36] in overall circuit configuration, where passive LC ladder structure is also used for the summation of each tap-delayed signals. Also, the new type of multiplier cell is proposed, which is modified from the conventional Gibert cell, to address any voltage headroom issues for 0.18 um CMOS technology. To the best knowledge of author, this is the first 0.18 um CMOS based equalizer IC for 10 Gbps data throughput over MMF.

This chapter is configured as follow:

First section will discuss the system level equalizer simulation for the MMF channel. The 500 m of MMF channel are measured with VNA and the measured S-parameters are converted to the time-domain impulse response, which is used to extract the optimum

number of taps and the tap coefficient values. System level equalizer performance results are presented by the eye diagram comparison and the modified channel impulse response by the equalization. The next section covers the circuit building block for the equalizer IC implementation. The newly proposed analog multiplier cell is described in detail with other types of multiplier cell. The passive LC ladder structure for artificial transmission line and the current summation nodes are covered. Finally the measurement results of the fabricated equalizer are presented.

4.1 SYSTEM LEVEL EQUALIZER SIMULATION WITH MMF

For the system level equalization simulation, the forward transmission characteristics of the MMF channel are measured via the VNA. For the comparison 100 m and 500 m length MMFs are measured respectively. The calibration for the fiber channel measurement is performed so that the S-parameter reference plane is set from the input of the VCSEL module to the output of the photoreceiver as shown in Figure 4.1.

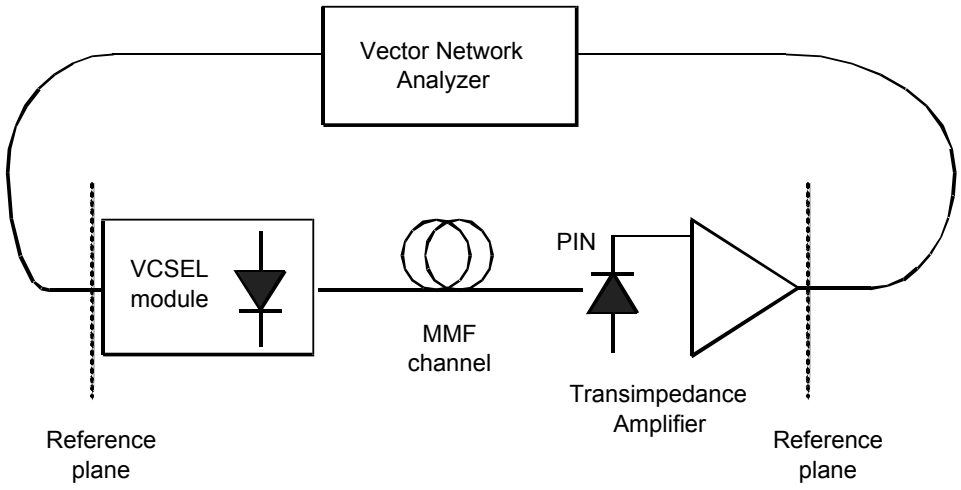
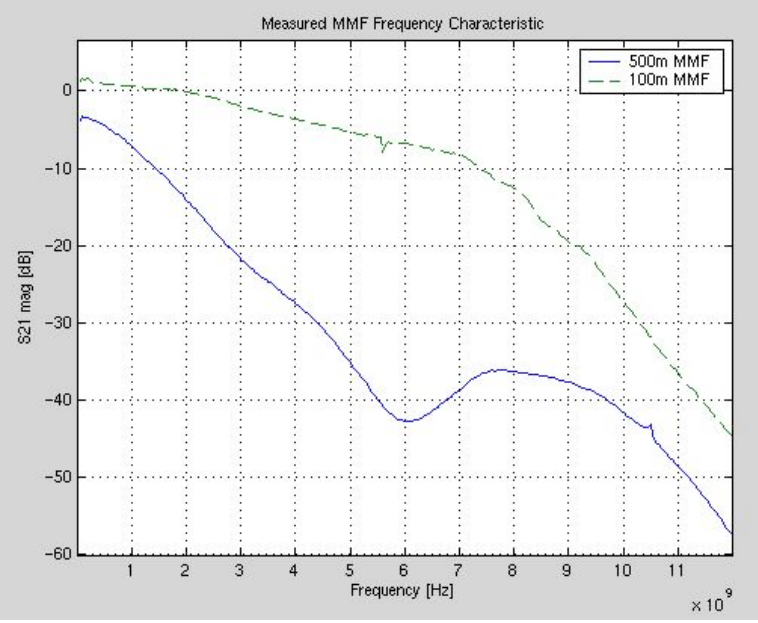


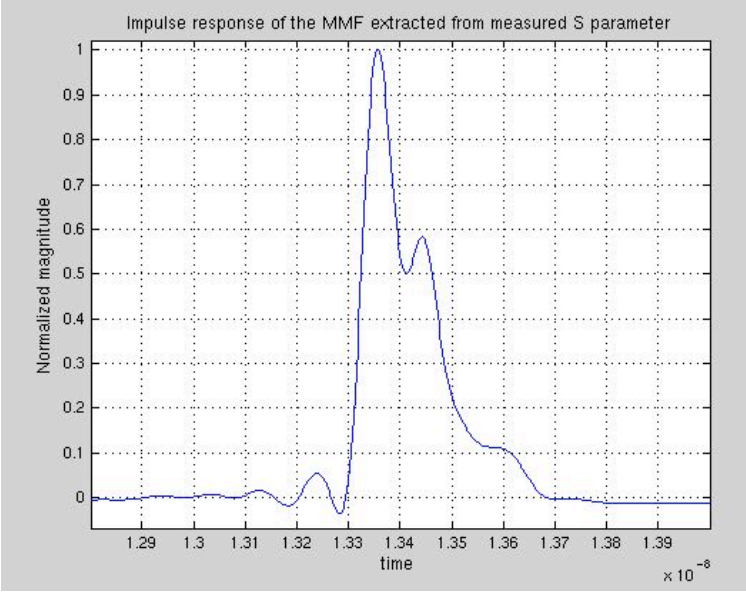
Figure 4.1. MMF channel measurement setup.

Figure 4.2 (a) shows the forward transmission characteristics of the MMF with different length respectively (100 m and 500 m). As it is expected, the 500 m MMF has more channel loss characteristics compared to 100 m MMF in the desired frequency band. The measured S-parameters are converted to an impulse response by inverse Fourier transformation. Figure 4.2 (b) shows the impulse response of the MMF channel. The second major mode is followed by the first major mode by around 100 ps, which is the symbol space for 10 Gbps data rate. The impulse response of the channel is used to extract the optimum equalizer specification. To optimize the tap coefficient values of the equalization, MMSE algorithm is adopted. The tap spacing for the 500 m MMF equalization is chosen as Ts/3, where the Ts is the symbol space for the desired data rate. For the 10 Gbps data throughput, the fractional tap space is specified to around 33 ps.



(a)

Figure 4.2. Channel measurement. (a) Measured forward transmission characteristic of 500 m multimode fiber. (b) Impulse response of the MMF channel.



(b)

Figure 4.2. Continued

The number of the taps is optimized as four. To implement the equalizer working with enough bandwidth for the given data rate, the number of taps are carefully chosen as small number as possible.

Figure 4.3 shows the impulse response of the 500 m MMF and the one modified by the equalization. The second major mode following the first major mode is attenuated almost by four times via the linear equalization. The normalized optimum equalization tap coefficient values for the 500 m MMF channels are: 1, 0.103, -0.085, and –0.442 from the first tap coefficient values to last tap coefficient values respectively.

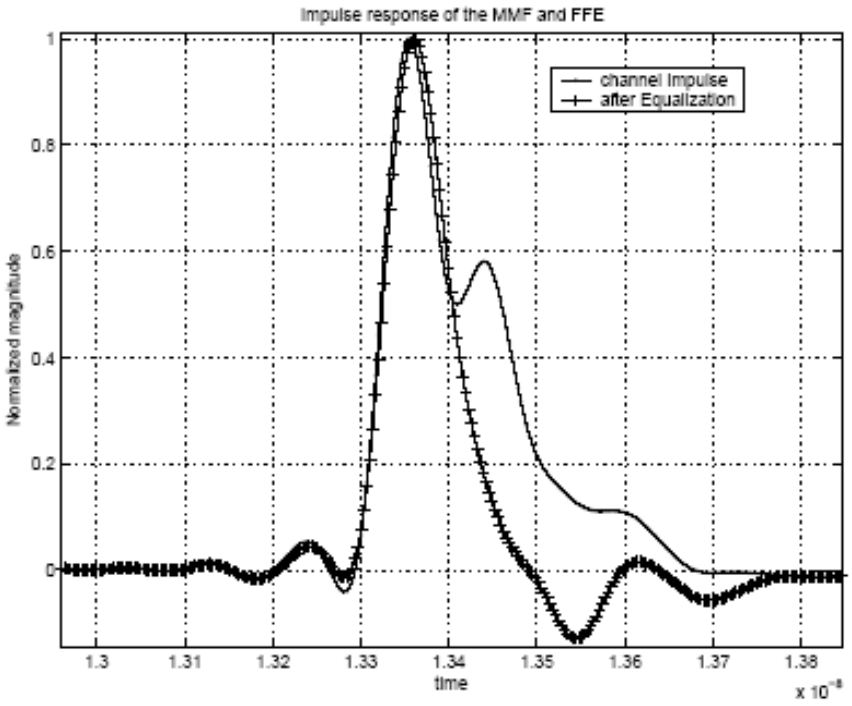
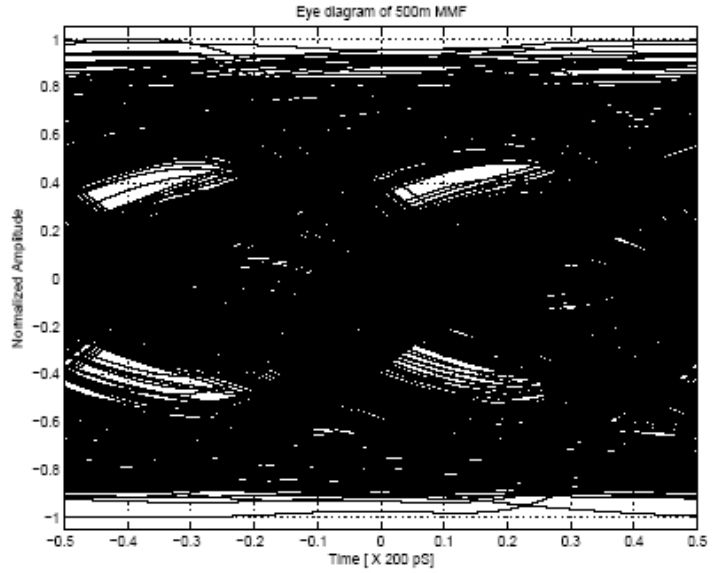
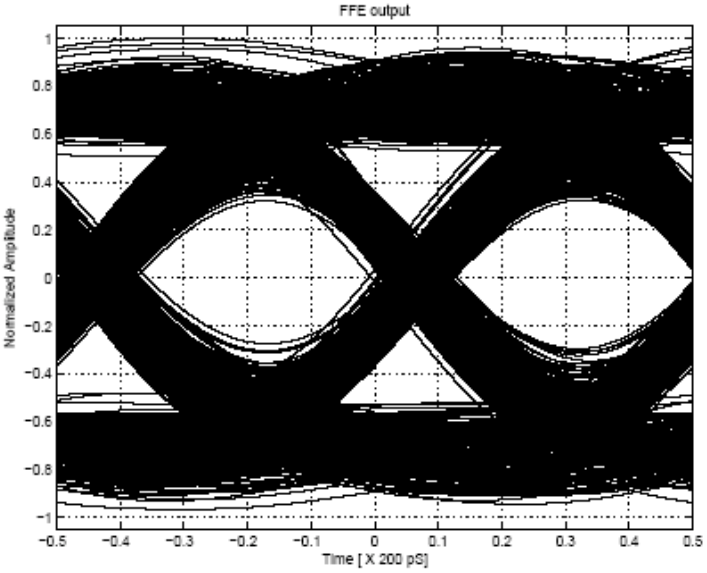


Figure 4.3. The impulse response of the channel and equalizer.

Figure 4.4 shows the eye diagram of the optical link probed at the output of the fiber before and after the equalization. The simulation is performed based on the measured MMF channel characteristics including the VCSEL module, 500 m length of the MMF, and the photoreceiver. The linear equalizer clearly improves the eye opening for 10 Gbps NRZ signal over the given channel.



(a)



(b)

Figure 4.4. Eye opening for the equalization. (a) Eye diagram after the 500 m MMF channel. (b) Eye diagram after the equalization.

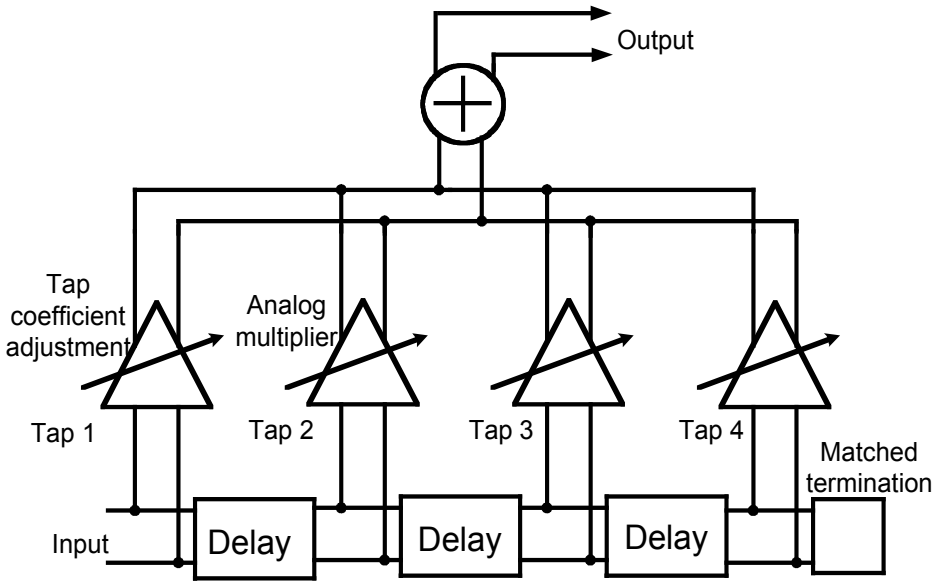


Figure 4.5. The FFE configuration with passive delay line.

The high-speed operation of the equalizer forces the circuit design as simple as possible. For this reason, the simple FIR structure is chosen as an equalizer at the receiver side. Considering the further adaptation and the voltage headroom limitation for the 0.18 um CMOS technology, the receiver side equalization is better choice over transmitter side equalization. The DFE is superior over linear FFE in equalization as mentioned in chapter 3. However the bandwidth issue on the subtraction node, where the signal from the FFE and the DFE is subtracted, made the FFE as a more practical choice over the DFE for the 10 Gbps data throughput operation. The overall circuit is implemented by the continuous time analog signal processing technique over the discrete time counter part, which requires the clock data recovery (CDR) block and the sampling circuitry. The continuous time analog signal processing technique makes it easier to operate in high data rate compared with the discrete time based equalizer because of the additional

circuitry required by discrete time counter part. The overall block diagram for the equalizer is shown in Figure 4.5.

In the following section, the building block for the equalizer implemented on a standard 0.18 um CMOS process will be discussed in detail.

4.2 CIRCUIT BUILDING BLOCK

In this section, the circuit building block for the equalizer will be discussed in detail. The multiplier cell will be covered first and the LC artificial delay line will then be discussed on the following section.

4.2.1 MULTIPLIER CELL

The Gilbert cell is conventionally used as a multiplier cell for the equalizer. The major function for the multiplier cell is to adjust the amplitude of the signal, which comes after the delay line cell. The most simple way for the gain variation is to control the bias current in the simple differential pair as shown in Figure 4.6 (a). The gain is proportional to the square root of a bias current from the small signal gain calculation. The current sink control method is simple to implement, however it still has undesirable characteristics such as the output common mode voltage variation depending on the gain. The other gain variation technique is to vary the degeneration resistor as shown in Figure 4.6 (b). The voltage gain for the source degenerated differential pair is

$$\frac{g_m}{1+g_m R_s} R_d$$

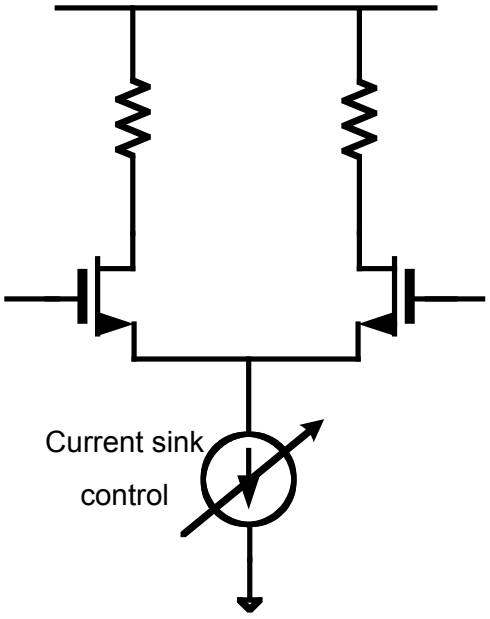
where g_m is the transconductance of the negative metal oxide semiconductor (NMOS), R_s is the degeneration resistance, and R_d is the load resistance. By changing the R_s, the overall voltage gain can be varied without changing the common mode output voltage. The variable resistor can be implemented by using on-resistance of the MOS.

The bias condition for the MOS to be used as a variable resistance is when the MOS operates in triode region (i.e. $V_{ds} > V_{gs} - V_t$, where V_{ds} is the drain-source voltage and V_t is the threshold voltage for the MOS). The on-resistance of the MOS is as follow:

$$R_{on} = \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{gs} - V_t)}$$

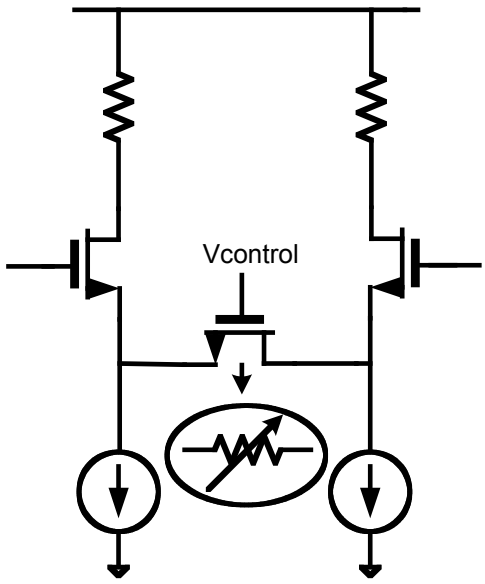
where μ_n is the mobility of the electrons, C_{ox} is the gate oxide capacitance per unit area, W is the MOS width and L is the MOS channel length.

By summary, the gain variation can be implemented by way of changing the bias current, degeneration resistance, or load resistance. However those methods are still not appropriate to be used for the multiplier cell because the multiplier cell needs bi-polar gain variation.



(a)

Figure 4.6. Gain variation for differential pair. (a) Differential pair with current sink variation. (b) Differential pair with source degeneration variation.



(b)

Figure 4.6. Continued

Therefore it is good idea to exploit the advantage of differential signaling, for example, the bi-polar gain is achievable by swapping the connection of differential pair. Figure 4.7 shows the two differential pair tied together at their drain with opposite signal polarity. This is called Gilbert cell. The bi-polar gain variation characteristic of the Gilbert cell makes it as a good candidate for analog multiplier cell. By this reason, the conventional Gilbert cell is considered as the multiplier cell for this equalizer design.

For high-speed circuit operation, passive loads are chosen over active loads as current summation node. However, despite the bandwidth advantage of the passive resistance loads, the open drain connection of the conventional Gilbert-multiplier cells to the resistive load results in a voltage drop across the passive load that increases linearly as the number of tap is increased (i.e. increased number of multiplier cell connection to the resistive load). This forces the transistors (M1, M2, M3 and M4) in Figure 4.7 to operate in the triode region.

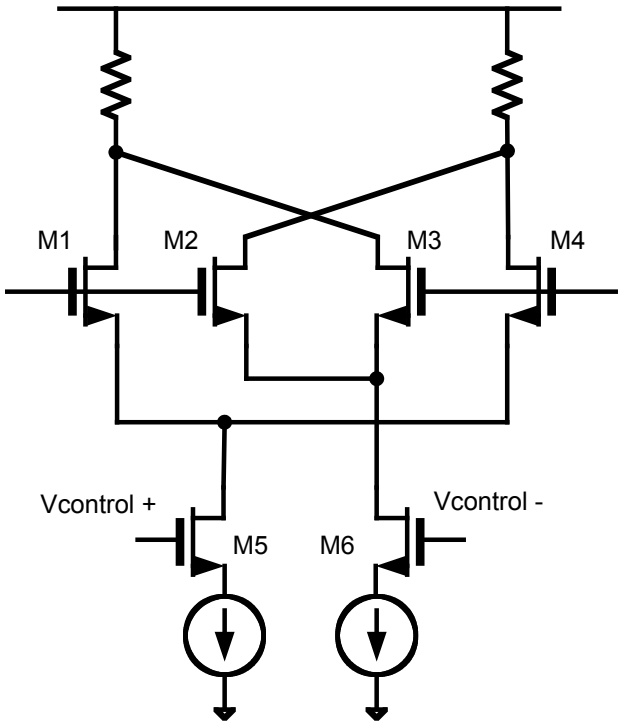


Figure 4.7. Gilbert cell topology.

To increase the available voltage headroom of the conventional Gilbert-multiplier cells, a modified Gilbert-cell is newly proposed in this research [48]. The cell architecture uses folded gain control circuit with the bias current block folded as well (shown in Figure 4.8). The mirror pole capacitance at the AC ground node resulting from the proposed cell has negligible effect on the overall bandwidth performance since the gain control signal path does not require the high bandwidth. Transistor M5, M6, M7 and M8 in Figure 4.8 are used for active degeneration in order to achieve high linear gain performance [50]. The gain control block includes a degeneration circuit (M11 and M12) for linear gain control as shown in Figure 4.8.

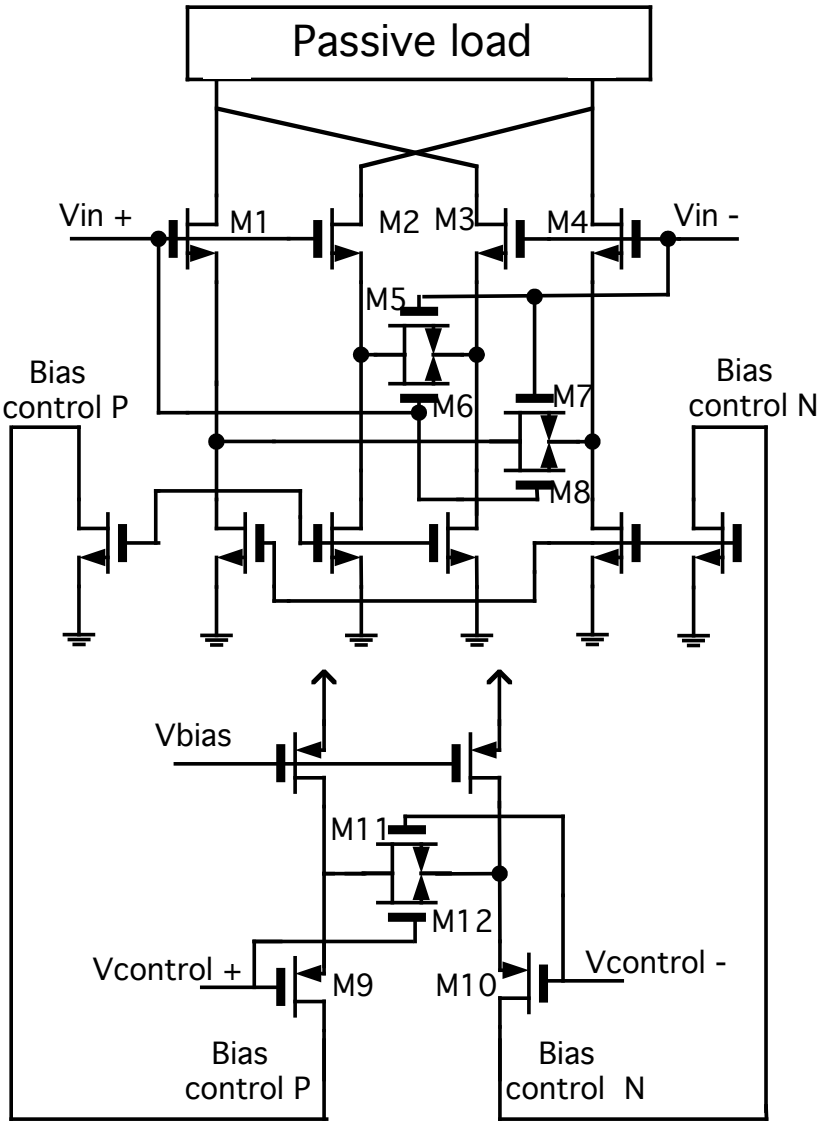
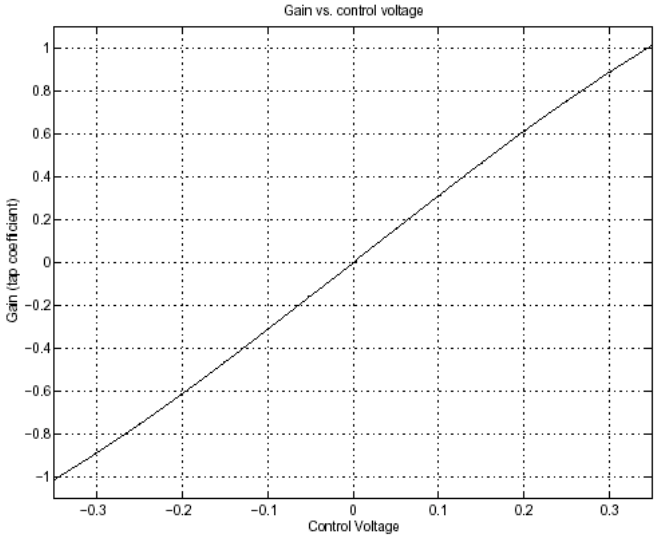


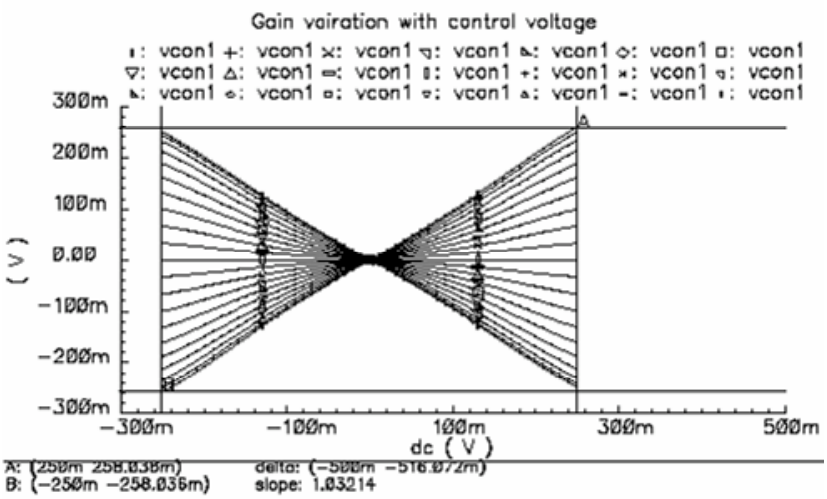
Figure 4.8. Modified Gilbert cell with folded gain control block.

The gain versus control voltage curve for the modified Gilbert cell structure is shown in Figure 4.9 (a) ensuring the linearity between the control voltage and the gain. Figure 4.9 (b) shows the DC gain curve of the multiplier cell structure demonstrating the maximum peak-to-peak input signal voltage level for its linear operation. The input

dynamic range is increased by use of the active source degeneration circuit (M5, M6, M7, and M8 in Figure 4.8).



(a)



(b)

Figure 4.9. DC gain characteristic of the modified multiplier cell. (a) DC gain variation vs. control voltage of the multiplier cell. (b) DC gain curve of the modified Gilbert cell showing input dynamic range.

Besides on this current steering technique, another way of implementing low voltage Gilbert cell operation is reported as shown in Figure 4.10 [51]. The gain variation by varying the degeneration resistance enables to remove the differential pair (M5, M6) in Figure 4.7. Replacing the three stacks of transistor to two transistor via source degeneration results in reduced voltage headroom consumption as well. The source degeneration variable resistance method has comparable voltage headroom consumption with the modified Gilbert cell structure because of identical number of transistor stacks. However, the method shown in Figure 4.10 has some potential gain symmetry problems. The MOS M5 and M6 have to have odd-symmetrical turn-on resistance relation, however the on-resistance has reciprocal relation to the gate voltage making it difficult to maintain odd-symmetry relation.

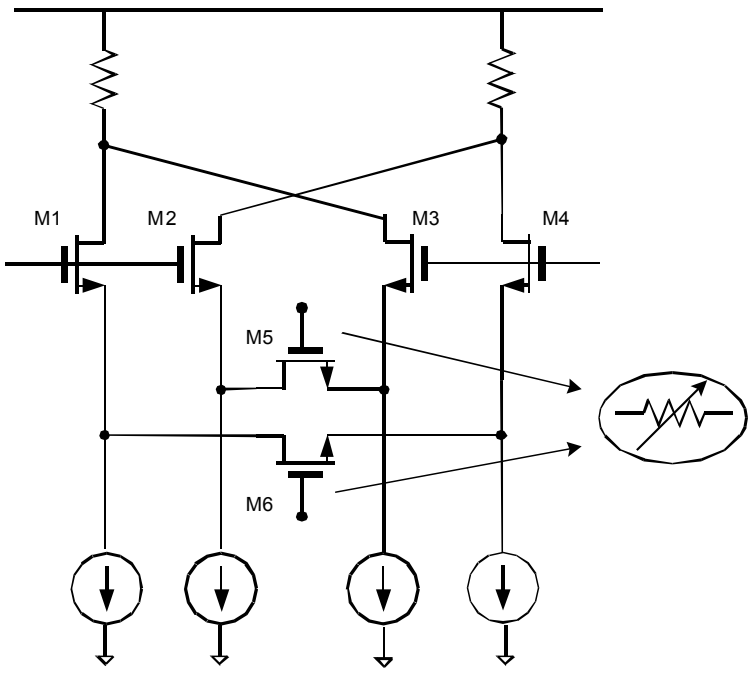


Figure 4.10. Gilbert cell with variable source degeneration.

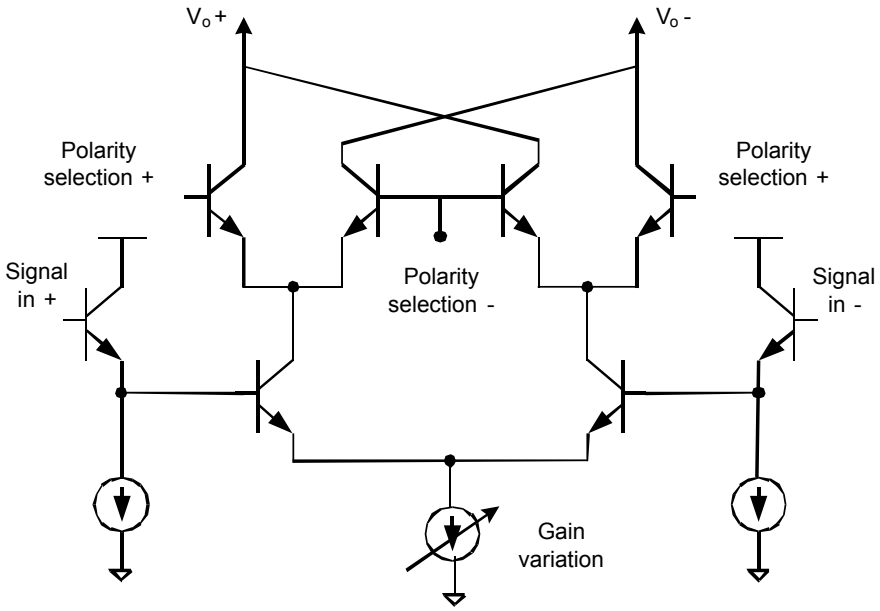


Figure 4.11. Gilbert cell using the upper transistor as switches.

Instead of using the upper four MOS (i.e. the M1, M2, M3, and M4 in figure 4.7) as the signal input, *H. Wu et al.* introduced the way using upper four transistors as switch to set the gain polarity and the current sink for gain variation as shown in Figure 4.11 [36]. This method has advantage that the output loading effect is minimized because two of upper four transistor is always on and the others are always off, which is independent of the gain value. However as mentioned earlier, current sink control method has potential undesirable effect that the output common mode voltage can be changed as the gain changes.

4.2.2 PASSIVE DELAY LINE

To meet the bandwidth requirement with the given CMOS technology (0.18 μm gate length), the distributed circuit design concept is adopted for this equalizer. The equalizer, which adopts the distributed-circuit concept is originated from the TWA, where the input and the output of the active device is connected by distributed passive network [36]. In this equalizer design, the distributed passive network is used for the continuous time analog signal delay. However, differentiating the design from the one in [36], the output of the each multiplier cell is current summed together by single passive load, not distributed passive network. The parasitic effects at the output node of the equalizer are minimized via optimizing the circuit design and high-speed layout technique.

The transmission line design is the most critical part for the distributed circuit design. For the equalizer design, the delay per stage is specified by 33 ps tap delay. Microstrip lines or coplanar waveguides would be too long to effectively implement this amount of delay on the silicon chip. For example, the simple calculation of the required physical delay line length is over 5 mm per stages. Considering these practical restraints, the continuous-time delay is implemented by the artificial transmission line, which is composed of inductor and capacitor ladder structure. The on-chip inductor with metal-insulator-metal (MIM) capacitor is used to implement the artificial transmission line. This lumped element approach is more practical on the limited chip space to generate the given amount of tap delay. Figure 4.12 shows the artificial transmission line used in this equalizer with the overall block diagram for the equalizer.

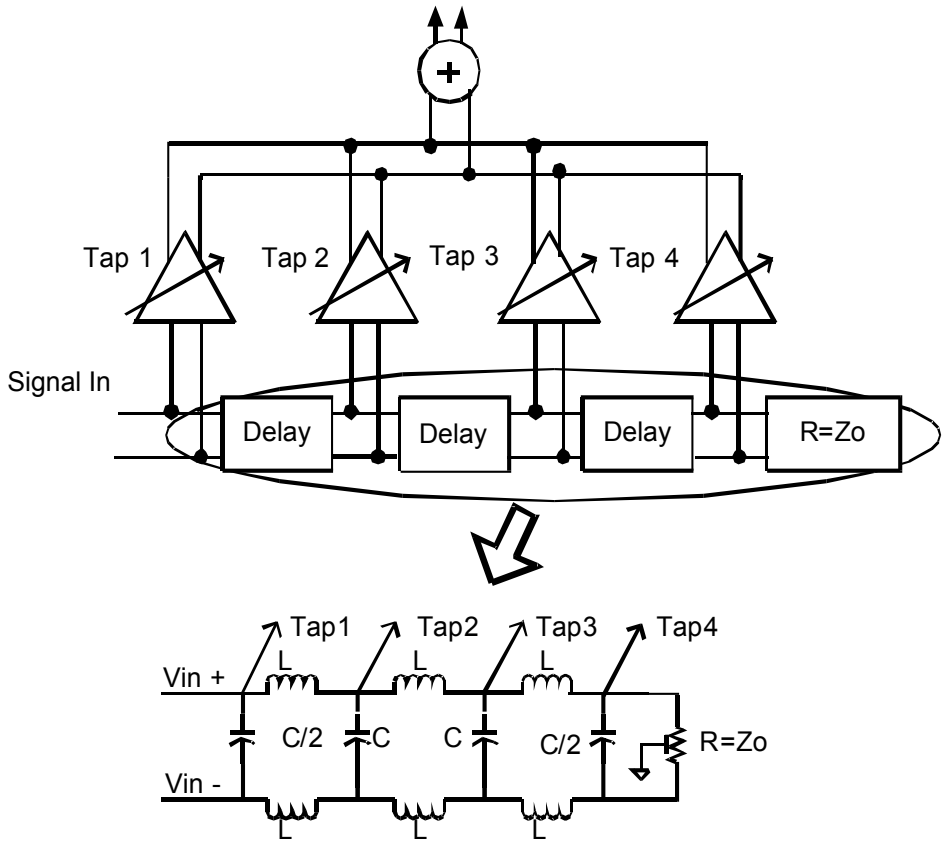


Figure 4.12. Artificial transmission line for the equalizer.

For the matched termination to the characteristic impedance of the artificial transmission line, there are several choices for the termination. For example, one choice is to end with a capacitance and terminate across it with a matched resistance. The other choice is to end with an inductance and terminate with matched resistance. Although both of termination works well, the better alternative is to use a half-section for the termination as shown in Figure 4.12. By using the half-section termination, the bandwidth for the artificial transmission line is increased further.

The artificial transmission line constructed by LC ladder is designed with 50 ohm differential characteristic impedance. This is achieved by appropriate choice of inductance, L_t and capacitance, C_t as shown in the following equation, where L_t and C_t are

the inductance and capacitance of each LC section. The characteristic impedance, Z_o and the time delay of each segment, T_{delay} is defined as follows,

$$Z_0 = \sqrt{\frac{L_t}{C_t}} \qquad T_{delay} = \sqrt{L_t \cdot C_t} \qquad (4.1)$$

The final capacitance values are optimized by considering all the input capacitance (Gate-to-Source capacitances) at each multiplier cell and the parasitic capacitance of the inductors. A 1.5 nH inductor is designed using Analysis and Simulation of Inductors and Transformers in Integrated Circuits (ASITIC) simulator and is implemented by optimizing the line space and number of turns to increase the self-resonance frequency of the inductor via enhancing the Q factor. As shown in Figure 4.12, the input impedance of the equalizer is matched to the characteristic impedance of the LC ladder, which is terminated differentially with 50 ohm resistors.

The lumped element analog LC delay line can work as transmission line below the cutoff frequency, however over this frequency the input impedance of the lumped LC line will be eventually pure reactive. The input impedance of the lumped LC delay line can be presented as equation (4.2).

$$Z_{in} = \frac{jwL}{2}\left[1 \pm \sqrt{1 - \frac{4}{w^2 LC}}\right] \qquad (4.2)$$

So the cutoff frequency, where the input impedance is purely reactive, is

$$w_{cutoff} = \frac{2}{\sqrt{LC}} \qquad (4.3)$$

From the simple calculation, we can verify that the lumped LC line has enough bandwidth to work as delay line for a given equalizer structure.

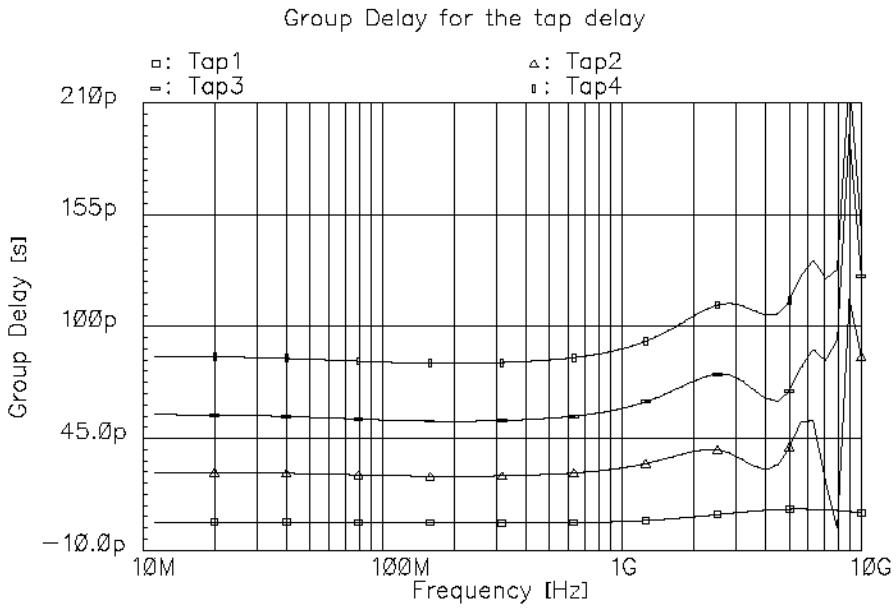


Figure 4.13. Group delay performance of the LC ladder structure.

The simulation result for the LC ladder structure is shown in Figure 4.13. The group delay performance for each tap is shown including the multiplier parasitic capacitance. The accurate methods to measure the tap delay performance is to measure the zero crossing point of the eye diagram by turn on the tap coefficient as one while all the others are set to zeros. This simulation is done by transient response engine in Spectres. Figure 4.14 shows the transient signal after the each tap delay, where four different time phase signal are plotted at the same time to measure the time delay. The zero crossing point for each adjacent signal is delayed by 33 ps.

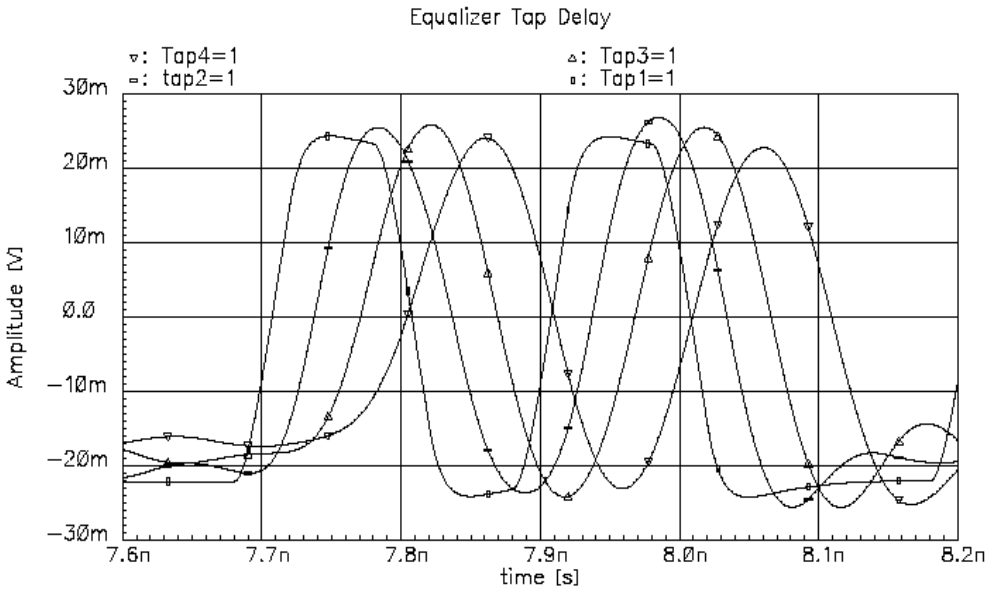


Figure 4.14. Eye diagram of the delay line showing the tap delay performance.

So far, the design of the equalizer is covered including the system level equalizer specification, multiplier cell structure, and the delay line elements. In the following section, the measurement result for this equalizer will be shown.

4.3 MEASUREMENT RESULTS

The equalizer to compensate the DMD dispersion is designed and fabricated on a standard 0.18 μm CMOS process. This section will cover the measurement result for the fabricated equalizer. First section will cover the measurement result for each building block such as the tap coefficient variation of the multiplier cell, bandwidth performance of the passive delay line structure. Also the tap delay performance of the passive LC ladder structure is shown. Finally the eye diagram before and after the equalization will be shown.

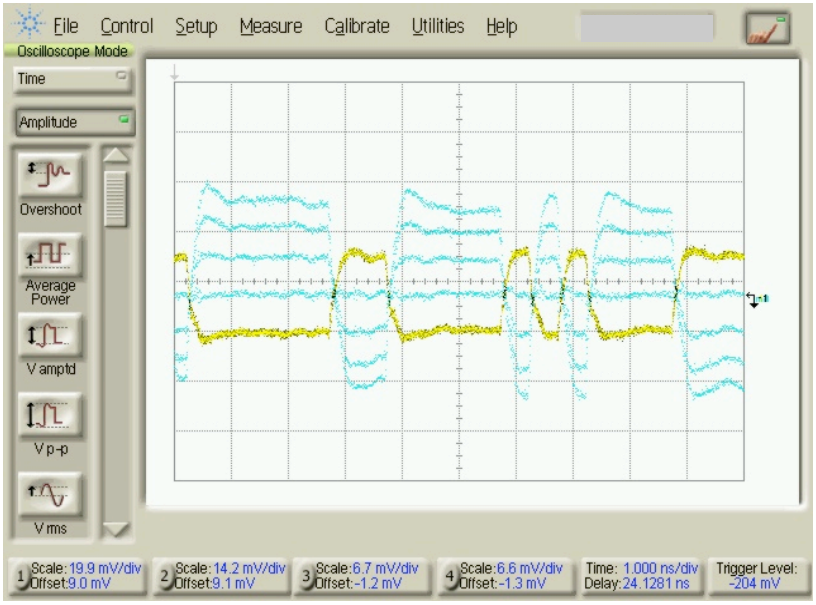


Figure 4.15. Tap coefficient variation of the multiplier.

Figure 4.15 shows the developed multiplier cell functional measurement results. A control voltage from 1.4 V to 700 mV is applied for tap coefficients variation. At the folded gain control block shown in Figure 4.8, we applied reference voltage of 900 mV at Vcontrol-, and control the voltage at Vcontrol+, which provides tap coefficient variation. For a clear view of the multiplier functionality, we applied 2 Gbps PRBS sequence in NRZ format as an input source directly to the equalizer input port.

Figure 4.16 shows the tap delay variation for the equalizer. The 10 Gbps on and off data pattern is generated and is fed to the equalizer. By putting the tap coefficient as one for the first tap coefficient, the zero delay signal output is measured. After that, the second tap coefficient is set to one, while all the others are set to zero, and measured the output of the equalizer. By this way, the tap delay measurement is done for the equalizer. Clearly, Figure 4.16 shows that each adjacent signal is delayed by around 33 ps through the passive LC network.

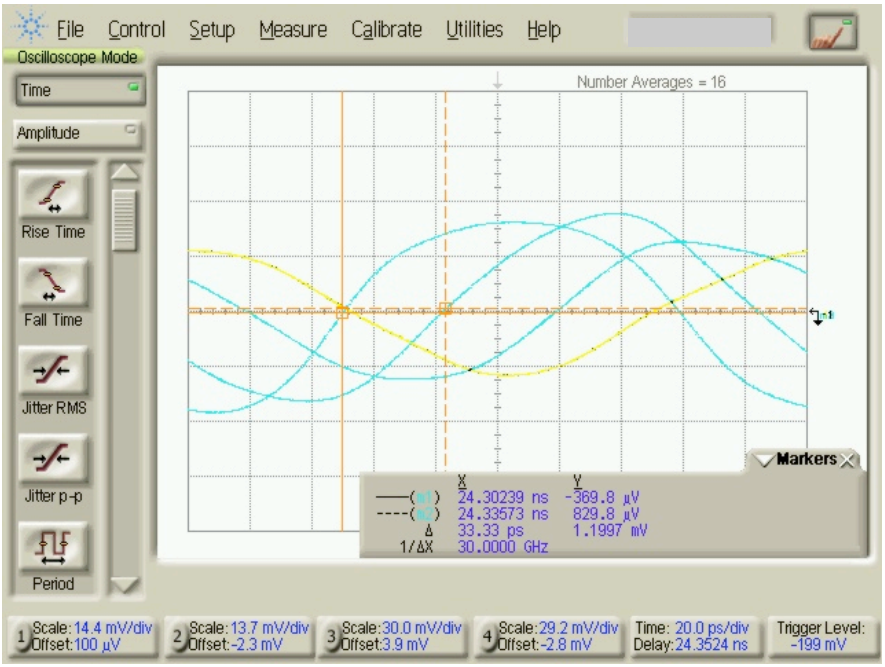


Figure 4.16. Tap delay measurement for the equalizer.

Figure 4.17 shows the measurement of the eye diagram for the passive LC delay line only. The 10 Gbps PRBS signal is fed to the equalizer and the last tap delay node is extended to the pad for the measurement purpose. The eye opening for the passive delay line shows that the passive delay line has enough bandwidth to transfer 10 Gbps NRG signal.

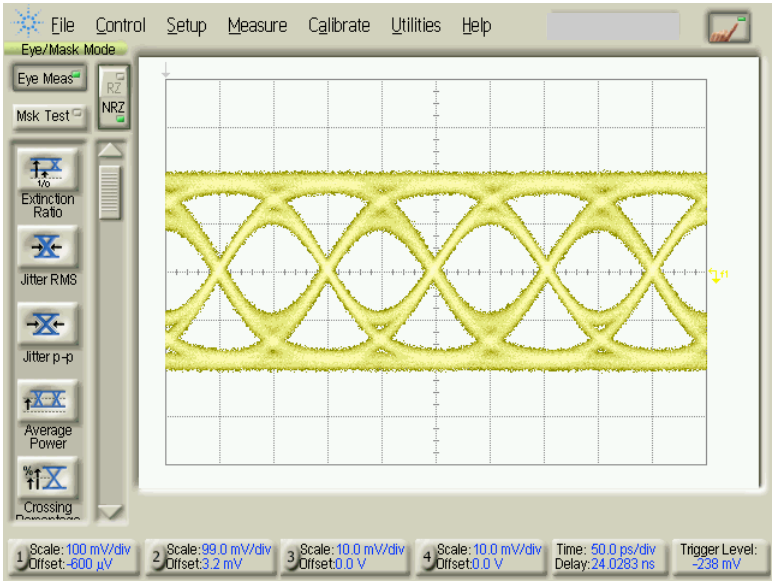
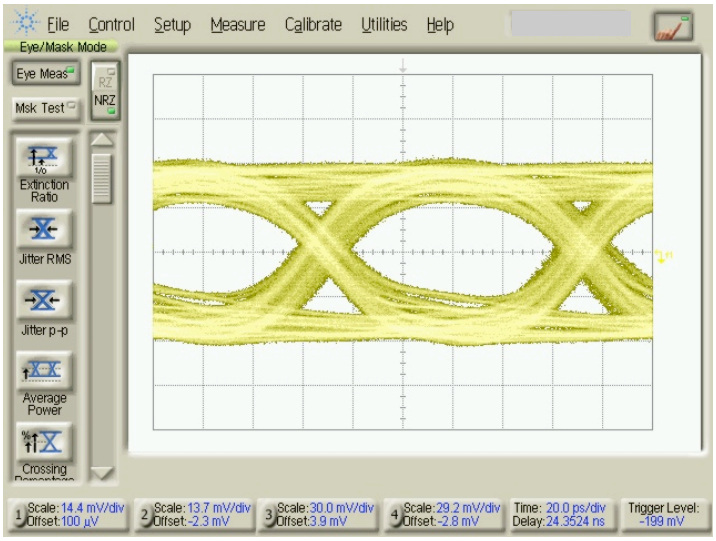


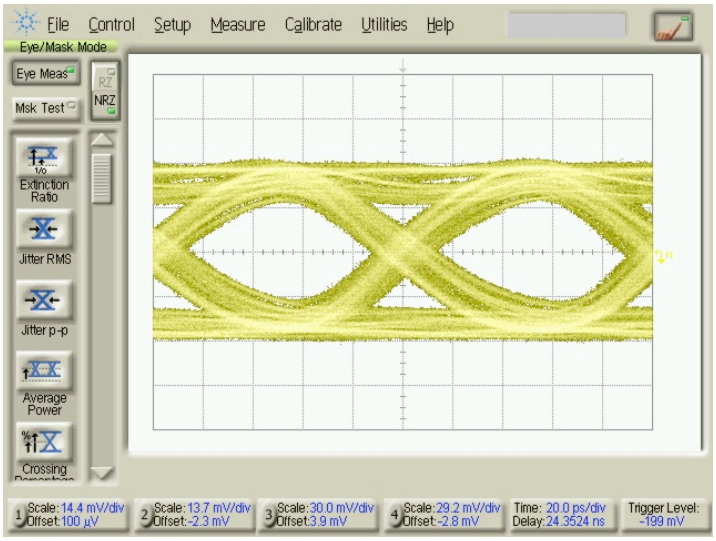
Figure 4.17. Eye diagram for the passive LC ladder structure.

Figure 4.18 a, b, c, and d shows the eye opening at the output of the equalizer when one of the tap coefficients are set to one while all the others are set to zero. The 10 Gbps PRBS signal is fed to the equalizer to ensure the bandwidth for the passive LC ladder and multiplier cell. The measurement method is identical to the tap delay measurement setup. The signal with the first tap as one has most broad bandwidth comparing with the other data path because it does not experience any time delay. As the signal passes further time

delay, the bandwidth also tends to be reduced as shown on the eye opening because the signal with the last tap set to one experiences most dispersion in passive LC ladder structure.

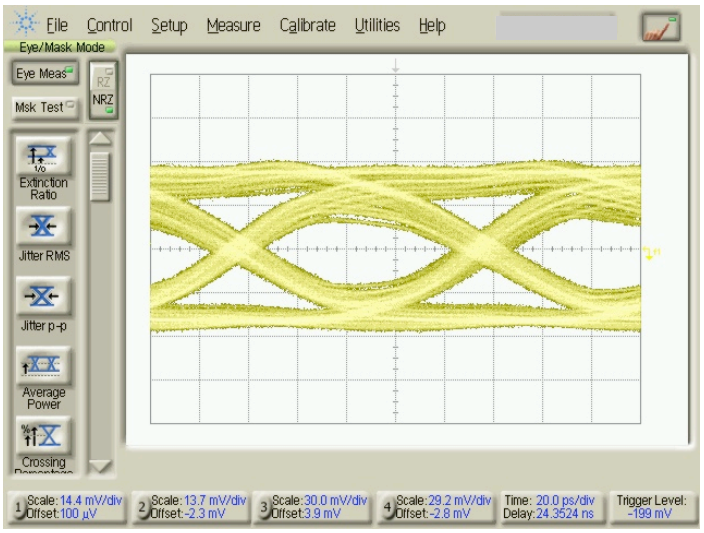


(a)

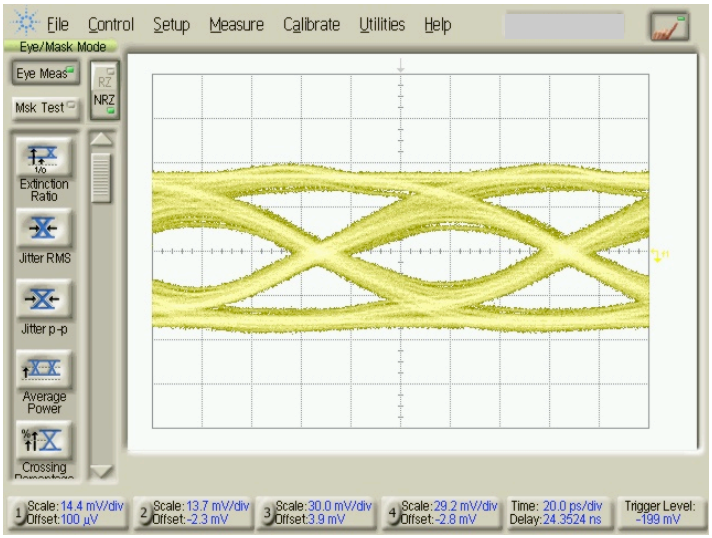


(b)

Figure 4.18. Eye diagram for (a)Tap1=1, (b)Tap2=1, (c)Tap3=1, (d) Tap4=1.



(c)



(d)

Figure 4.18. Continued

Figure 4.19 shows the measurement setup for the equalizer with the MMF and the optical transceiver module. The VCSEL module including integrated VCSEL is used as the transmitter. The 500 m length MMF with the core size of 62.5 μm is used as the fiber channel. The photoreceiver module is used as a receiver. Due to the single-ended scheme for the optical communication system, the balun is inserted between the photoreceiver and the equalizer to convert the single ended to differential signal. The balun used for the measurement has the 3 dB bandwidth more than 10 GHz ensuring no undesirable signal distortion on the balun.

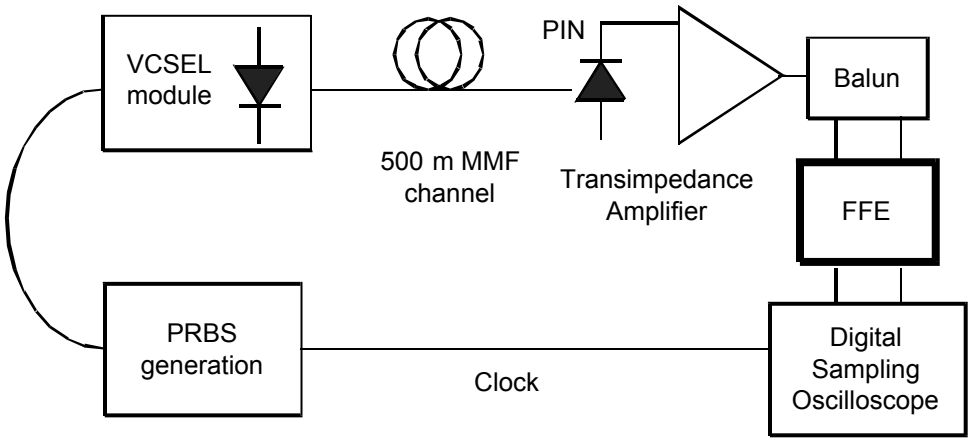
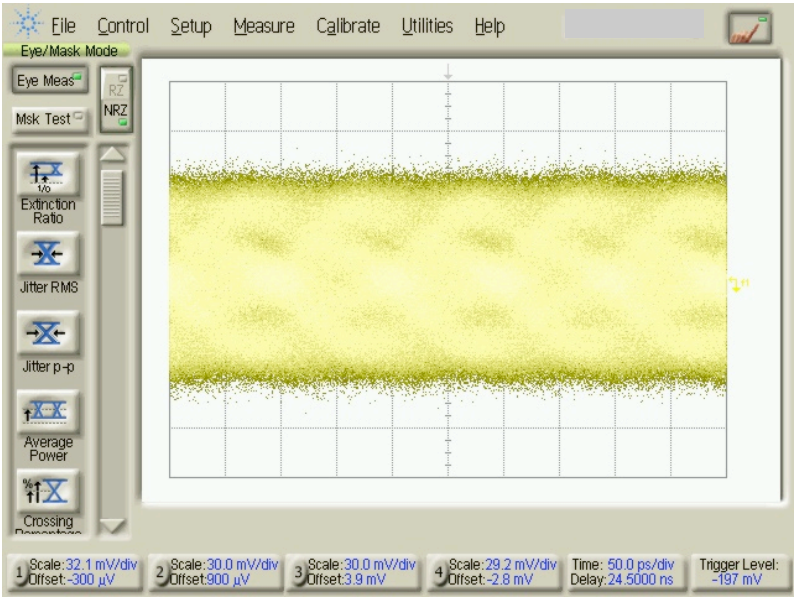


Figure 4.19. Measurement setup for the equalization.

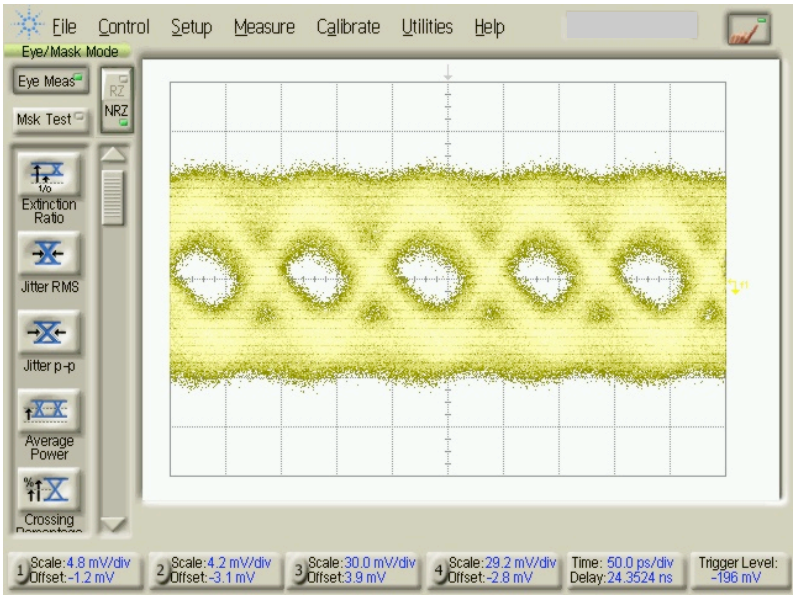
Finally Figure 4.20 shows the eye diagram of the signal before the equalization and after the equalization. The 10 Gbps PRBS data sequence is generated from the bit error rate test (BERT) equipment and transmitted to the VCSEL module. The signal goes through the 500 m MMF channel and received with the photoreceiver and converted to the differential signal by the balun. The eye diagram in Figure 4.20 (a) shows the signal

distortion because of the DMD effect in the 500 m MMF. With the equalizer, the distorted signal is rebuilt as shown in Figure 4.20 (b). The peak-to-peak voltage after the equalization is around 60 mV differential. Overall current consumption for the equalizer is 4.5 mA with 1.8 V power supply voltage. Even though the initial tap coefficients values are optimized from the system level simulation, additional tap coefficient adjustment is required because the system level simulation does not count on the signal loss from the passive tap delay line. By reversely scaling the loss coming from the each tap delay, the tap coefficient compensation is performed manually to optimize the eye opening after the equalization.



(a)

Figure 4.20. Eye opening for the equalization. (a) Before the equalization. (b) After the equalization



(b)

Figure 4.20. Continued.

Figure 4.21 shows the microphotograph of the fabricated equalizer chip. The overall chip size is 1.09 mm by 1 mm.

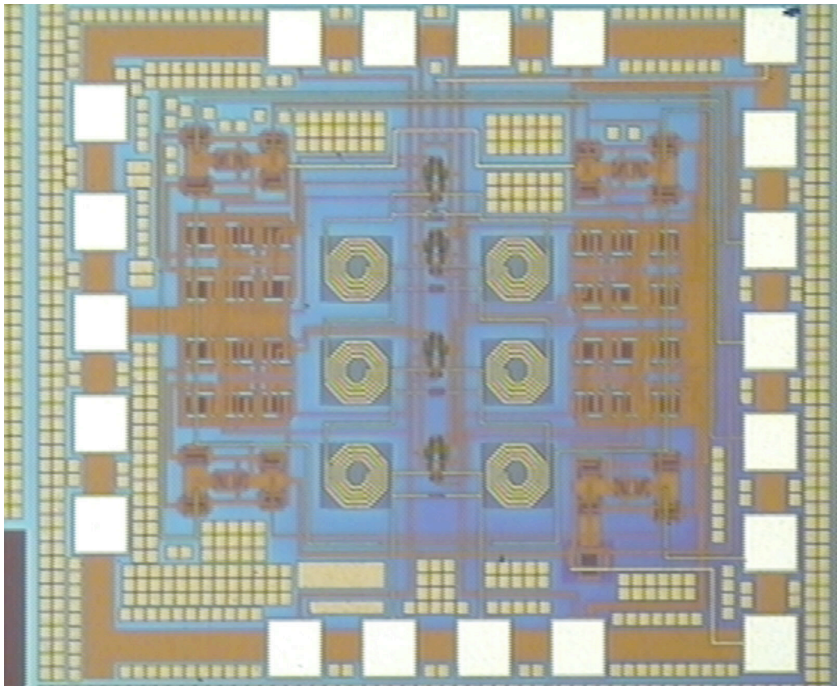


Figure 4.21. Photograph of the FFE chip.

The passive delay line based equalizer is designed and measured for the optical application. Eventhough the distributed LC network provides broad-bandwidth characteristic for high-speed signal operation, it still consumes large die area. Also design of the artificial transmission line is restricted by the available inductor models, which is vulnerable to the process variation. In the next chapter, the equalizer based on the active delay line will be described.

CHAPTER V

FFE WITH ACTIVE DELAY LINE

In this chapter, the continuous time equalizer with the delay line composed of active components is described. The active delay line means the delay line composed of active circuit components in this thesis. The main structure of the equalizer is identical to the one described in the previous chapter. However, from an implementation point of view, the equalizer described in this chapter adopts the active delay line differentiating it from the passive LC ladder type approaches. It is mentioned previously that the distributed circuit has intrinsic broadband characteristic. Despite the advantages of broad bandwidth characteristic for the distributed circuits, there are several undesirable factors that the passive LC ladder approaches have. The artificial transmission line, which composed of passive on-chip inductors and MIM capacitors still require more space than the one with the active delay line structure. The process variation of the CMOS technology is inevitable on the passive LC ladder structure. Because the delay line is implemented by passive LC network, it is difficult to make any variable delay to compensate any process variation effects. Also the passive delay line has AC signal loss characteristics per each tap delay, which requires additional tap values adjustment. Based on these several facts, it is desirable to implement the FIR type equalizer with active delay line.

The most challenging part in active delay line design is to satisfy the bandwidth requirements for 10 Gbps signal operation by overcoming the intrinsic narrow bandwidth characteristic of the active delay line compared with its passive counter part. So it is required to have any bandwidth enhancement method for the delay line.

In this thesis, the active delay line based equalizer with active inductance peaking approach for its delay line is introduced. Compared with the RC delay approach, where differential pair with passive load is used, this approach adds additional zeros in frequency domain generating peaking at the high frequencies. Therefore the 3 dB bandwidth of the active inductance peaking approach is extended over the one without peaking. This is the first 0.18 um CMOS equalizer with active delay line approach for 10 Gbps data operation over 500 m MMF.

In the following section, the active delay line based equalizer configuration will be described. Also on the building block sections, each circuit block will be covered in detail. In the last section, the measurement result with 500 m MMF including the optical transceiver will be presented.

5.1 EQUALIZER CONFIGURATION

The equalizer is the FIR type of structure with 4 tap coefficients and $T_s/3$ fractional tap spacing. All 4-tap coefficients are derived from a MMSE algorithm and 33 ps of delay per stage is adopted for the fractional-spaced equalization as mentioned previously. In the equalizer IC implementation point of view, the equalizer has a single to differential converter at the front end to interface with photoreceiver output. The single to differential

converter is inserted to convert the single ended output signal of the photoreceiver to differential input signal to the FIR structure in equalizer. A broadband buffer stage is at the output of the FIR structure for low voltage differential signaling (LVDS) level signal transition to external 50 ohm termination. The active delay line is composed of four unit delay cell. Each unit delay cell is composed of two cascaded NMOS differential pair with the NMOS source follower configuration as a load to ensure the acceptable bandwidth for 10 Gbps data rate. The NMOS source follower load is used to emulate the inductance at the desired frequency range, therefore generating zeros adjacent to the most dominant pole of the unit delay cell.

Figure 5.1 shows the block diagram of the overall equalizer integrated on a single chip. All the building blocks are integrated with 0.18 μm standard CMOS process.

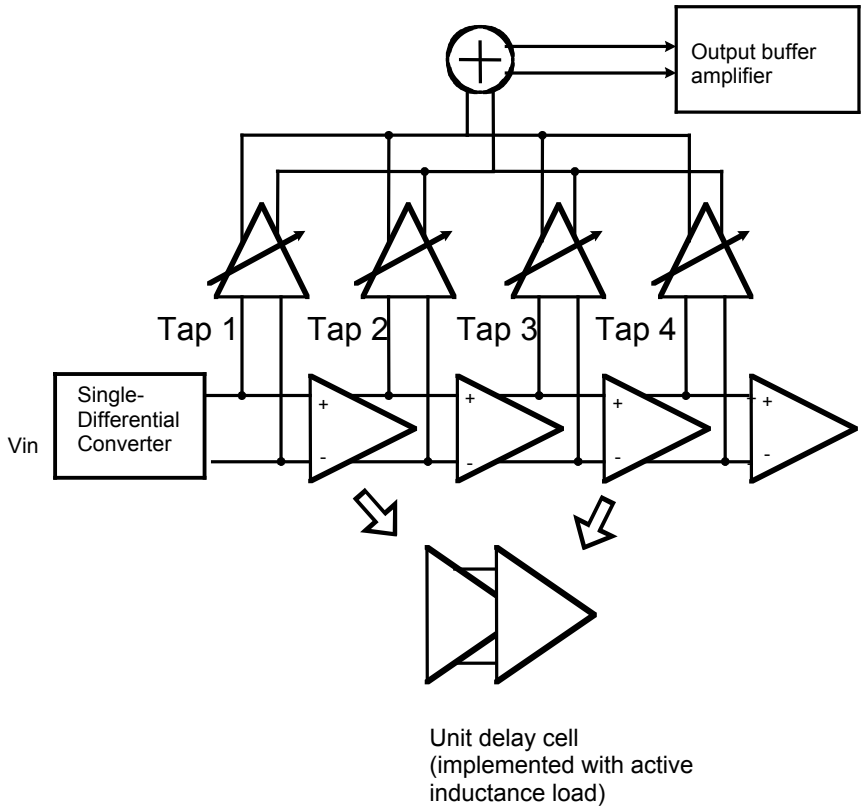


Figure 5.1. Fully integrated equalizer configuration.

5.2 BUILDING BLOCK

In this section, each circuit building block for the equalizer will be described in detail. In the first section, the single to differential converter block will be covered with the design consideration. In the following section, power supply noise immune bias method will be discussed. The active delay line circuit design is described in the next section including various broadband circuit design examples. Finally the output buffer of the equalizer, which is composed of five differential pair stages will be studied.

5.2.1 SINGLE TO DIFFERENTIAL CONVERTER

The single to differential converter is required to convert the single-ended optical data arriving at the input of high-speed photoreceiver into differential signals to drive fully differential equalizer circuits. At the high-speed operation necessary in optical link, the architecture employing the differential signal scheme is better choice over single-ended scheme because of the enhanced common mode noise rejection ration and the reduced signal logic swing, which in turn reduces the required voltage headroom. However, the single-ended scheme in optical communication is preferred because the fully differential operation of the optical link requires more optical components, which is usually bulky and expensive over electrical channel.

Broadband passive balun is one of the good candidates for single to differential conversion. The balun is the microwave components which receive the signal and outputs two signal with 180 degree phase difference. However the broadband passive

implementation on a silicon substrate to cover multi-GHz frequency range is very challenging due to the required space and the silicon substrate loss characteristics.

In this thesis, the single to differential converter is implemented with a NMOS differential pair, a source follower, and a buffer stage as shown in Figure 5.2. Signal input port is biased by resistor circuitry emulating 50 ohm input impedance. The other port of the differential pair is biased to the reference voltage, which is identical potential to the input DC voltage level. Any asymmetry effect due to the different signal path in the differential pair is compensated in the source follower stage and the following buffer stage. Figure 5.3 shows the input and output 10 Gbps PRBS bit stream of the single to differential converter.

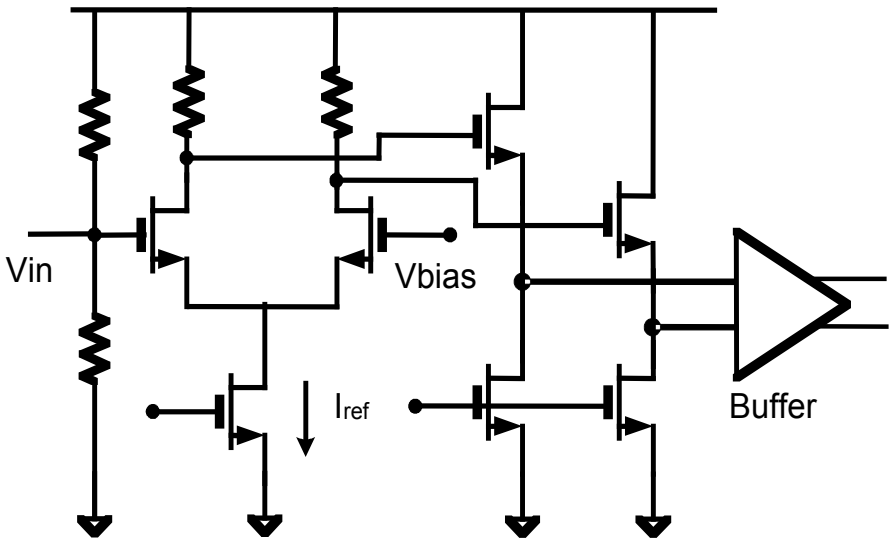


Figure 5.2. Single to differential converter.

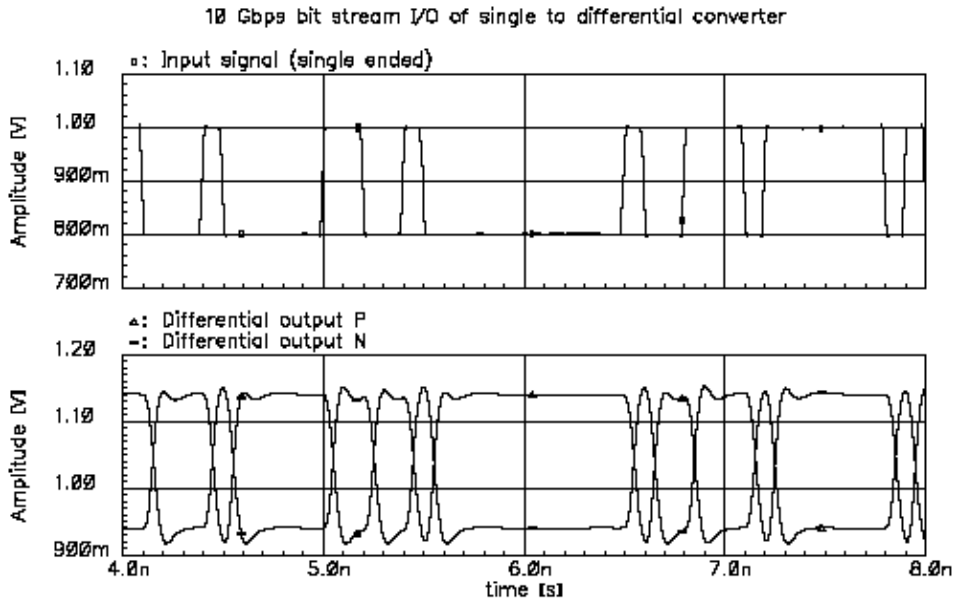


Figure 5.3. Input and output 10 Gbps bit stream of the single to differential converter.

5.2.2 POWER SUPPLY NOISE IMMUNE BIAS SCHEME

The reference current source is generated using the supply noise rejection enhanced bias scheme as shown in Figure 5.4 [52]. For a given ΔV_{dd}, the ΔV_{ref} is as follow:

$$\Delta V_{ref} = (\Delta V_{dd} - \Delta V_{pmos}) \frac{Z_2}{Z_1 + Z_2}$$

As a result, the sensitivity of the V_{ref} to V_{dd} is reduced by a factor of ΔV_{dd}-ΔV_{pmos}. Therefore the reference current I_{ref} is $\frac{V_{ref}}{R}$, where R is the resistance connected to the source of the NMOS. As a result, the reference current sensitivity to V_{dd} is also reduced with a same scaling factor as V_{ref} to V_{dd}.

This improved noise immune reference current is used for all the equalizer building block including the single to differential converter, unit delay line cell, multiplier cell, and the output buffer stages. The reciprocal relation between the reference current and the resistance reduces any undesirable resistance variation effect on a differential pair where the current sink is mirrored with reference current and passive resistance is used as a load. The improved noise rejection from the power supply (V_{dd}) reduces the tail current noise in the delay line cell as well. As the time delay is proportional to 1/gm of a NMOS load in unit delay line cell, it alleviates any time delay jitter coming from the power supply noise in the delay line cell.

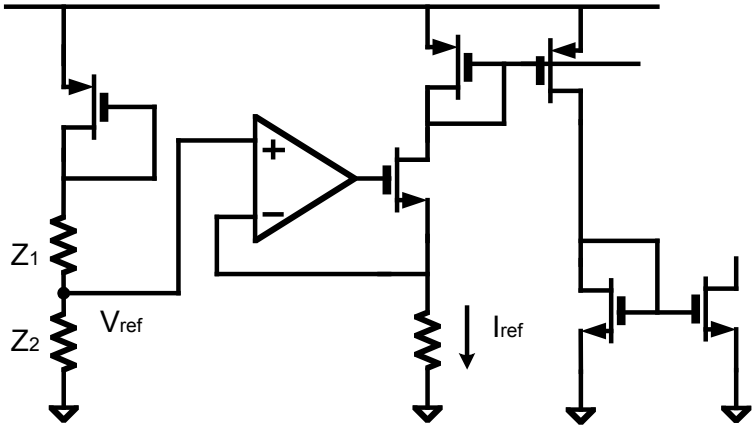


Figure 5.4. Noise rejection enhanced bias scheme.

5.2.3 ACTIVE INDUCTANCE PEAKING DELAY LINE

The equalizer introduced in chapter 4 uses passive LC ladder emulating the transmission line as the continuous time delay elements to ensure the broad bandwidth. However as it is mentioned, the passive delay is vulnerable to the process variation. Also it requires large CMOS area, and suffers from limited design freedom because of the 50 ohm characteristic impedance matching requirements, thus limiting the choice of usable on-chip inductors. By these reasons, this chapter introduces the active version delay line. However, it is more challenging to satisfy the bandwidth requirements for 10 Gbps signal handling over the passive delay line counter part. In this section, the various bandwidth enhancement methods will be covered briefly and the active inductance approach will be presented.

The most well-known bandwidth enhancement technique is to use shunt peaking inductor at the signal path. Figure 5.5 shows the example for inductive peaking technique. Series connection with the resistor R_d generates zero at R_d/L in frequency domain. By controlling the inductance value the frequency peaking range can be determined. This technique is used widely however it still have some disadvantage that it have to use on-chip inductors.

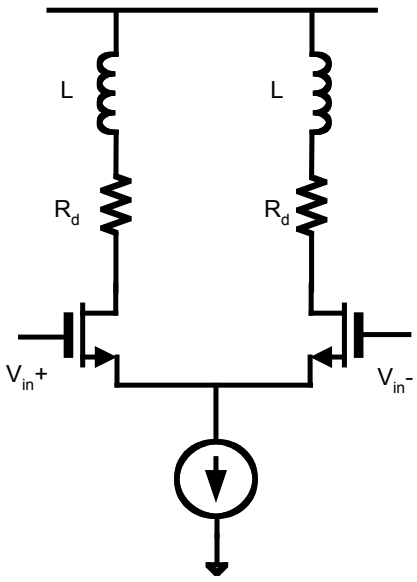


Figure 5.5. Peaking inductance to enhance the bandwidth.

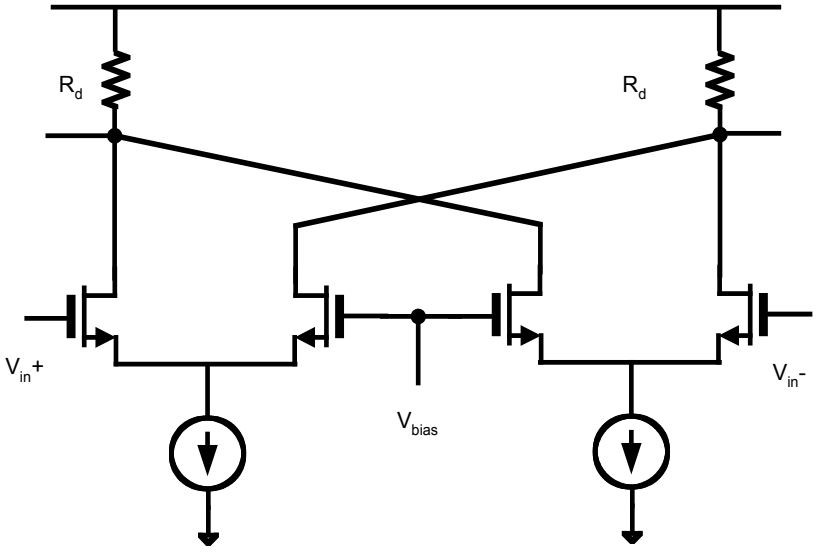


Figure 5.6. F_t doubler.

Another bandwidth enhancement technique is to add the capacitance in series with the input gate-source capacitance. Therefore, the input capacitance of the given stage can be

reduced by half. The one example of this technique is shown in Figure 5.6, where two differential pairs are connected in series at the input and in parallel at the output port. The overall voltage gain is still same as the single differential pair, however the input capacitance is reduced by half (C_{gs} /2, where C_{gs} is the gate-source capacitance of four NMOS in two differential pairs). Because the circuit structure has the half input capacitance, it is called F_t doubler [53]. Eventhough the reduced input capacitance advantage, this structure has several drawbacks compared with the simple differential pair. The overall power consumption is doubled because of using additional current sink. The current flow at the resistive load is increased by double, increasing the voltage drop, which tend to force the four NMOSs in two differential pair working in triode region. Therefore, this structure has reduced output voltage swing and the reduced input dynamic range. Finally, the C_{ds}, and C_{gd} of the current sink transistor is not negligible increasing the input capacitance from the ideal value of C_{gs} /2. Despite these drawbacks, the F_t doubler is widely used in high-speed buffer stage.

In order to create broadband characteristic, it is possible to degenerate the transistor in a way to increase their transconductance as the operation frequency is increased. Therefore, it compensates the high-frequency roll-over resulting in increased bandwidth. Figure 5.7 shows the one example of capacitive degeneration in differential pair. Using the half circuit of the Figure 5.7, the voltage gain is:

$$A_v = \frac{R_d \left\| \frac{1}{sC_L} \right.}{\frac{R_s}{2} \left\| \frac{1}{2C_s s} + \frac{1}{g_m} \right.}$$

$$= \frac{g_m R_d (sC_s R_s + 1)}{(1 + sR_d C_L)(g_m R_s / 2 + 1 + sC_s R_s)}$$

The voltage gain has zero at the $1/C_sR_s$ and two poles at $1/R_dC_L$ and $[g_m R_s/2+1]/C_sR_s$. By controlling the degeneration capacitance C_s, the peaking can be located at the desired frequency or cancel the dominant pole resulting in increased bandwidth.

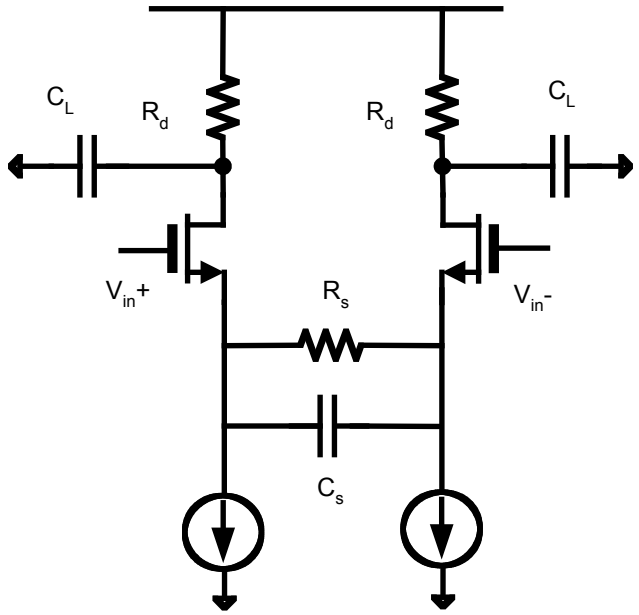


Figure 5.7. Capacitive degeneration.

Finally, the Cherry-Hooper amplifier is studied as a broadband characteristic circuitry [54]. Figure 5.8 shows the example of the Cherry-Hooper amplifier with ideal current source as the load. From the simple calculation, the voltage gain for the Cherry-Hooper amplifier is

$$g_{m1}(R_d - \frac{1}{g_{m3}})$$

Therefore as far as $R_d >> 1/g_{m3}$ the overall voltage gain is same as simple differential pair. However the output impedance of the Cherry-Hopper amplifier is approximately

$1/g_{m3}$, which is usually smaller than MOS drain resistance r_d resulting in output pole location much far from the origin compared with the simple differential pair. Eventhough the broadband characteristic of the Cherry-Hopper amplifier, more current consumption compared to the simple differential pair is the drawback of the Cherry-Hooper amplifier.

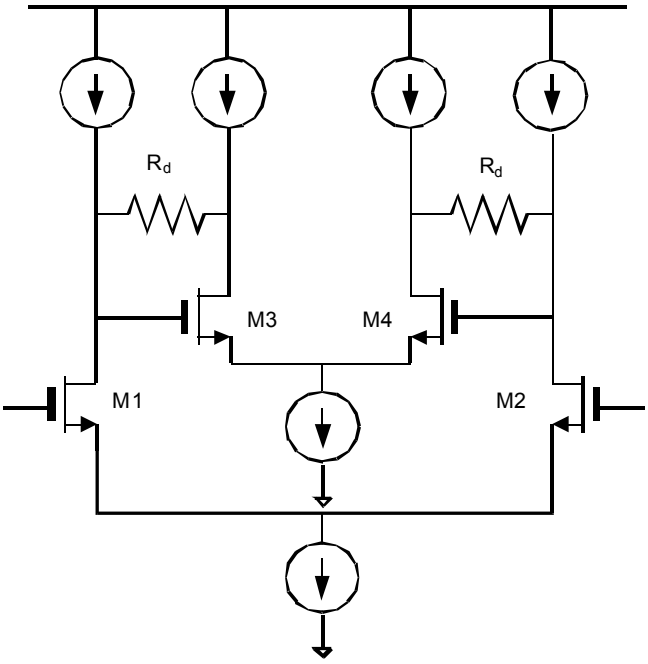


Figure 5.8. Cherry-Hopper amplifier.

So far, various type of broadband technique has been introduced, which is available in conventional CMOS technology. For the active delay line, shunt inductance peaking method is chosen because the power consumption compared to the other techniques are minimum. However as it is been mentioned, the on-chip passive inductor is still requiring large CMOS chip space, which is identical disadvantage to passive LC delay line approaches. To integrate further and implement a various time delay, the author chooses

the source follower as a load replacing the series combination of on-chip inductor and resistor.

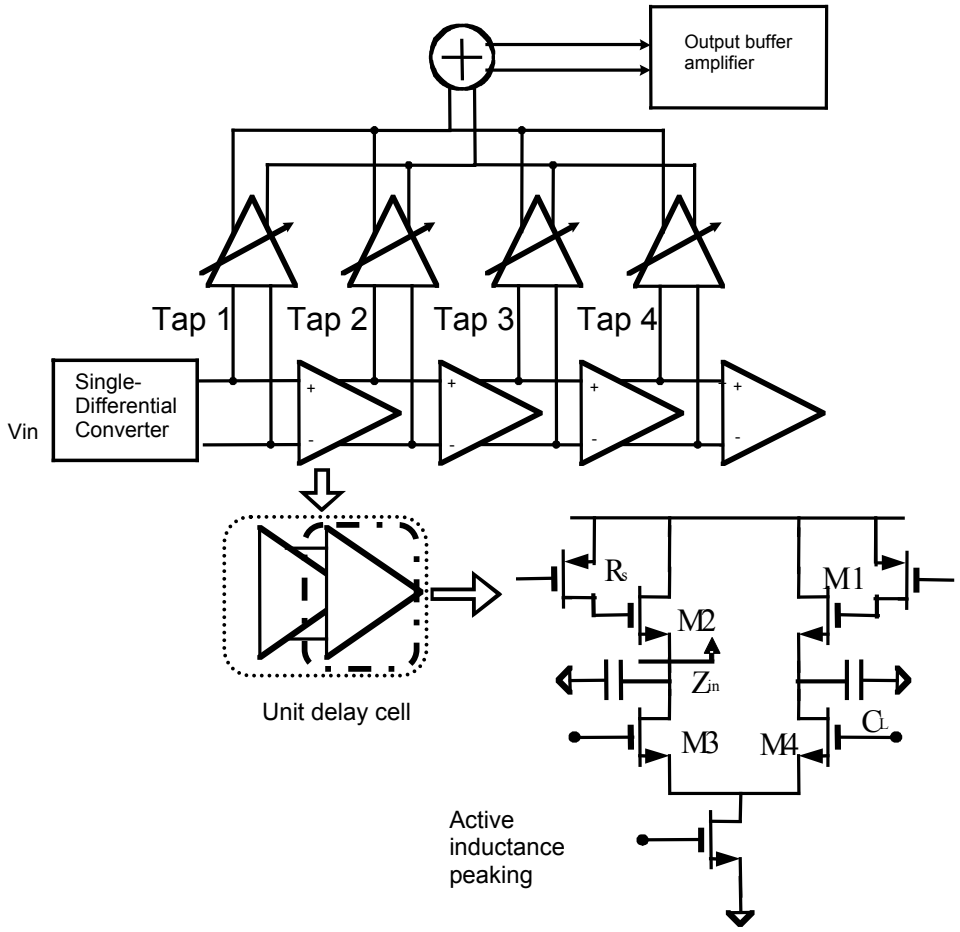


Figure 5.9. Fully integrated equalizer structure with active delay line structure.

Figure 5.9 shows the active delay line cell with overall equalizer structure. The overall voltage gain for differential pair in unit delay cell is

$$A_v = g_{m3} \cdot (Z_{in} // C_L)$$

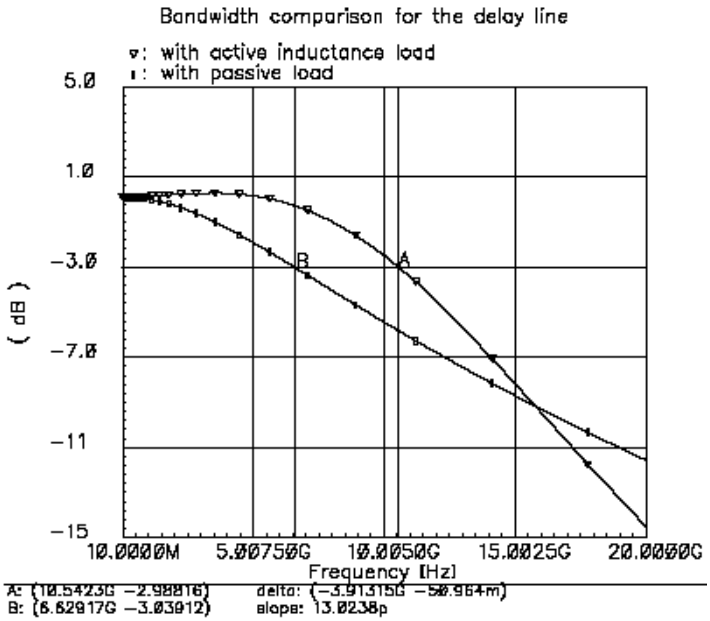
$$= \frac{sC_{gs2}R_s g_{m3} + g_{m3}}{C_{gs2}C_L R_s s^2 + (C_{gs2} + C_L)s + g_{m2}}.$$

where $C_L = C_{gd3}(1 + A_v) + C_{db3}$, and

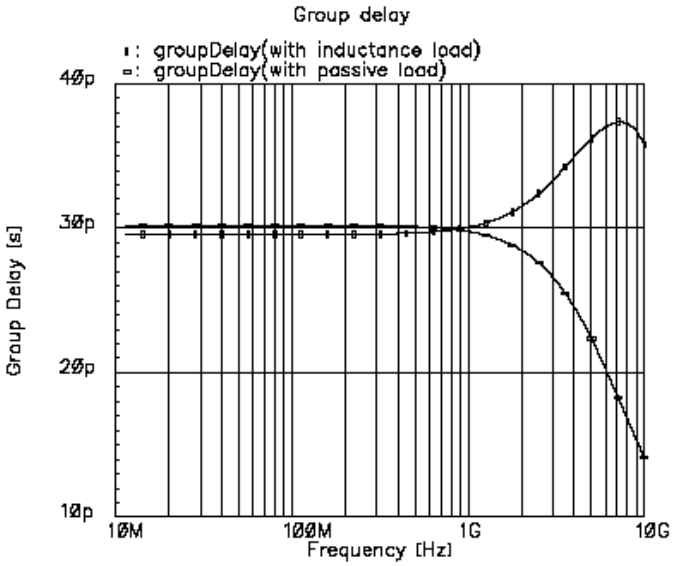
$$Z_{in} = \frac{sC_{gs2} \cdot R_s + 1}{sC_{gs2} + g_{m2}}.$$

The two poles are at $-\frac{1}{2}(\frac{C_{gs2} + C_L}{C_{gs2}C_L R_s}) \pm \frac{1}{2}\sqrt{(\frac{1}{C_L R_s} + \frac{1}{C_{gs2}R_s})^2 - \frac{4g_{m2}}{C_{gs2}C_L R_s}}$ and the zero is at $\frac{1}{R_s C_{gs2}}$. By varying the R_s, (R_s is turn on resistance of M1 in Figure 5.9.) the zero location can be controlled. To reduce the external voltage source for the equalizer, turn-on resistance is replaced by passive resistance in this design. Figure 5.10 shows the bandwidth comparison between the active delay line composed of differential pair with passive resistor load and the one with active inductance load. The peaking adjacent to the dominant pole enhances the 3 dB bandwidth of the delay line by approximately 3.9 GHz compared with the delay line with passive resistor load. For the fair comparison, the group delay for the passive resistor load and the active inductance load is simulated with same amount of value. Also the gain for the delay line is optimized as one for both cases. The simulation includes all the parasitic capacitance from the multiplier cell and the adjacent delay cell.

For the active delay line implementation, two cascaded NMOS differential pairs are used generating 33 ps ($T_s/3$) delay per unit delay cell. The effective inductance value, which is proportional to $R_s/(1/g_{m2})$, is optimized for 10 Gbps NRZ signal transmission. Figure 5.11 shows the transient simulation result for the equalizer. The relative delay between the taps are optimized to around 33 ps.



(a)



(b)

Figure 5.10. Bandwidth comparison between the passive load and active inductance load. (a) The 3 dB bandwidth comparison between passive load and active inductance load. (b) Group delay for the passive load and active inductance load.

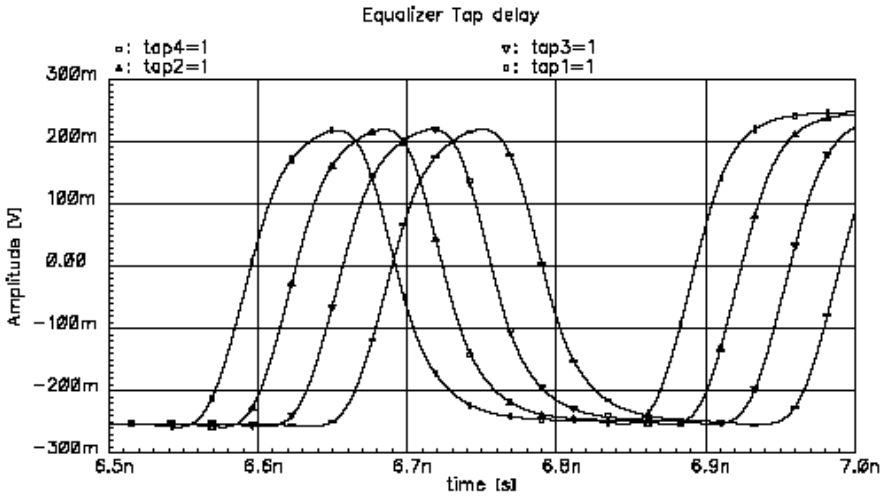


Figure 5.11. Delay line performance with 33 ps continuous time tap delay.

5.2.4 OUTPUT BUFFER STAGE

Five cascaded differential pairs are used for the output buffer stage as shown in Figure 5.12. Instead of using identical gain cell for all five stages, first and last stages use different topology compared with the second, third, and fourth stages. The each stage except first and last, also adopted the inductive peaking technique to ensure the required bandwidth. The first stage uses the simple differential pair with passive load because of the high common mode voltage level at the input of the output buffer. The last stage is implemented with passive load as well to increase the slew rate by flowing large signal current swing and to secure large signal swing level.

A voltage signal swing level at the input stage of the buffer stage eliminates the need of offset compensation because the input swing level is large enough compared with the input offset voltage level.

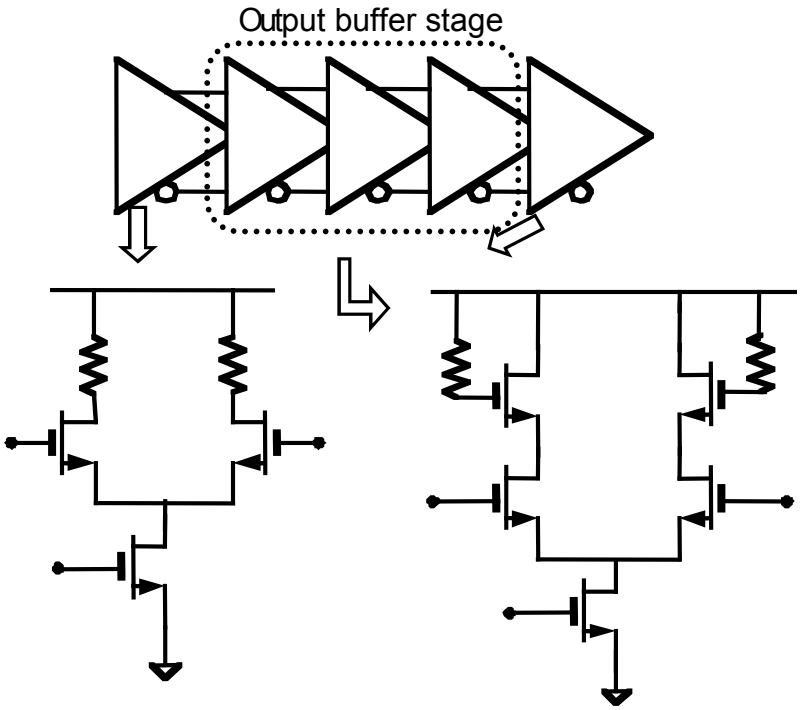
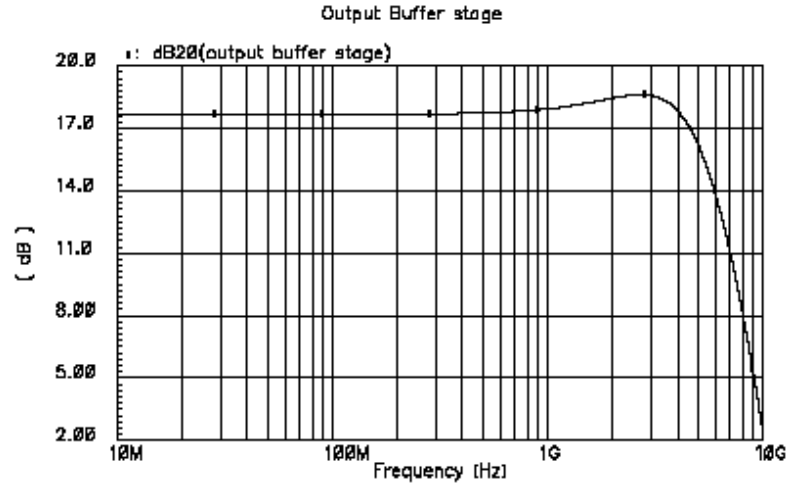


Figure 5.12. The output buffer structure.

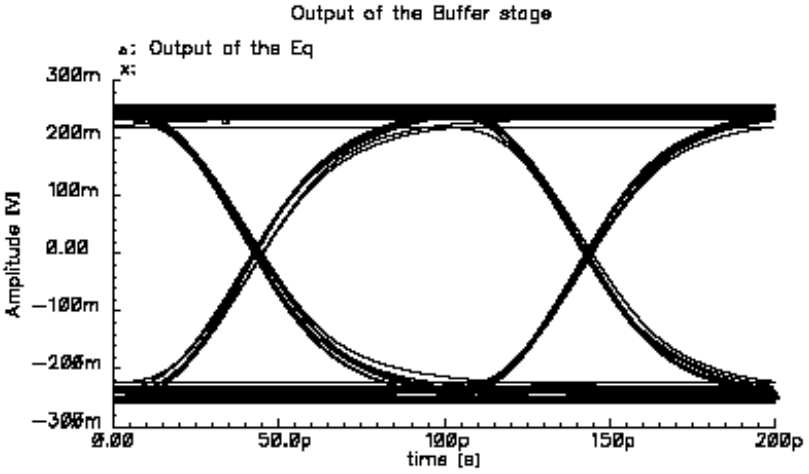
Figure 5.13 shows the high-speed operation characteristic for the output buffer stage considering the output impedance of the previous FIR structure. The 3 dB bandwidth for the output buffer stage is shown in Figure 5.13 (a). As the fourth and fifth stage in the buffer structure is operating more in switching mode, the 3 dB bandwidth of the overall stage is not so meaningful compared the one used for delay line design. However it is still valuable in design purpose.

The design is finalized in time domain transient response simulation to ensure the eye opening. Figure 5.13 (b) shows the time domain simulation result with 10 Gbps PRBS signal at the input of the equalizer. The eye diagram is captured at the output buffer stage

showing enough high-speed performance for the output buffer. The output voltage swing satisfies the LVDS swing level with the 50 ohm external termination.



(a)



(b)

Figure 5.13. High speed performance of the output buffer stage. (a) Frequency response for the output buffer stage. (b) Eye opening at the output of the equalizer through the buffer stage.

5.3 MEASUREMENT RESULT

The electrical performance of the equalizer is measured without optical link before the equalization measurement is performed. As we have shown the performance of the multiplier cell in the previous chapter, the delay line performance of the equalizer is shown in this chapter.

Figure 5.14 shows the measured response of the equalizer showing the delay line performance used in this equalizer. The step signal is used as an input signal source. The output of the step signal going through the different data path is shown in figure 5.14. Each data path is the result of the one tap coefficient being set to one while all the others are set to zero. The plot shows 33 ps tap delay through the active delay line cell.

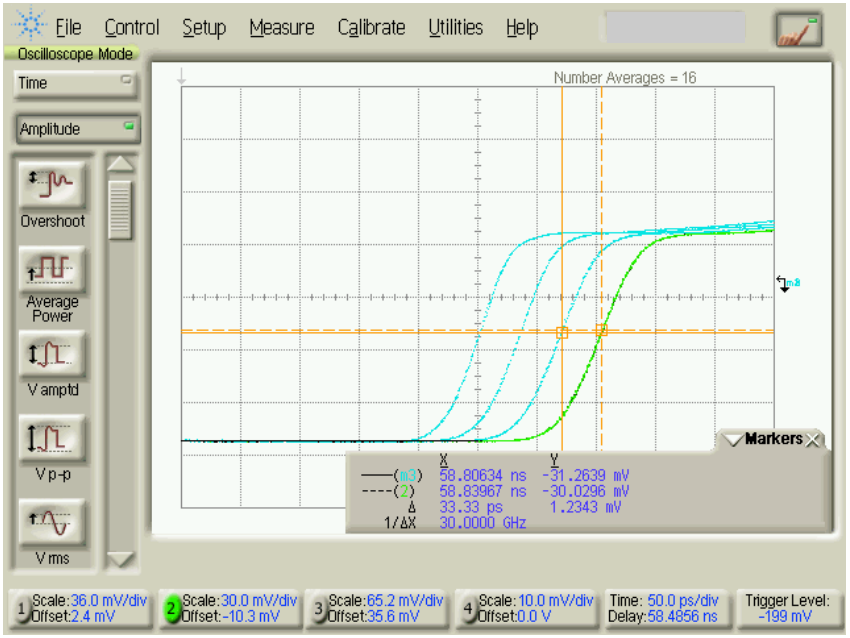


Figure 5.14. Measurement result of the 33ps tap delay with pulse train input signal.

To measure the equalization over the MMF link, the measurement setup is prepared as shown in Figure 5.15. Similar to the setup made for the LC delay line based equalizer, the optical link with 500 m of 62.5 μm core-size MMF is used. Also the VCSEL (λ=850 nm) module and the photoreceiver complete the MMF optical link. Right after the photoreceiver, the active delay line based equalizer is connected directly

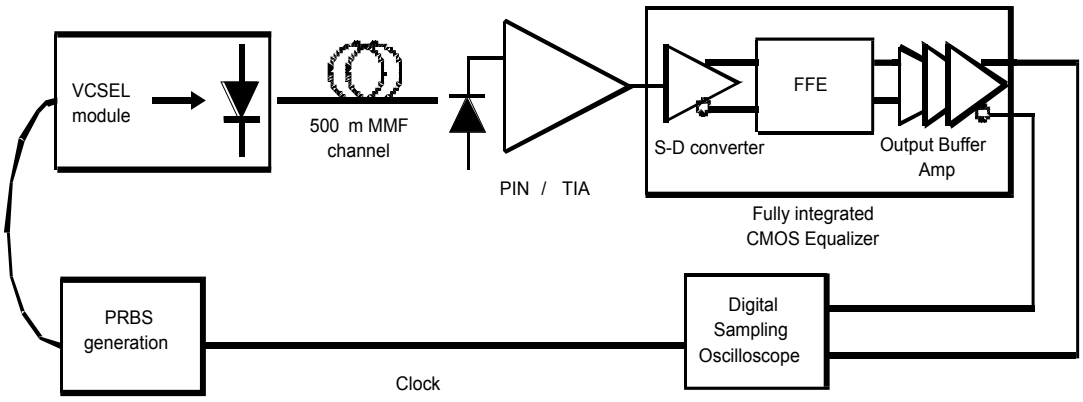
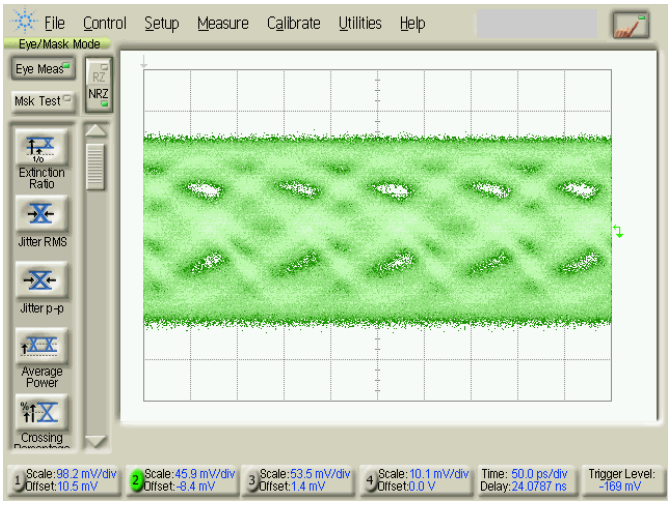
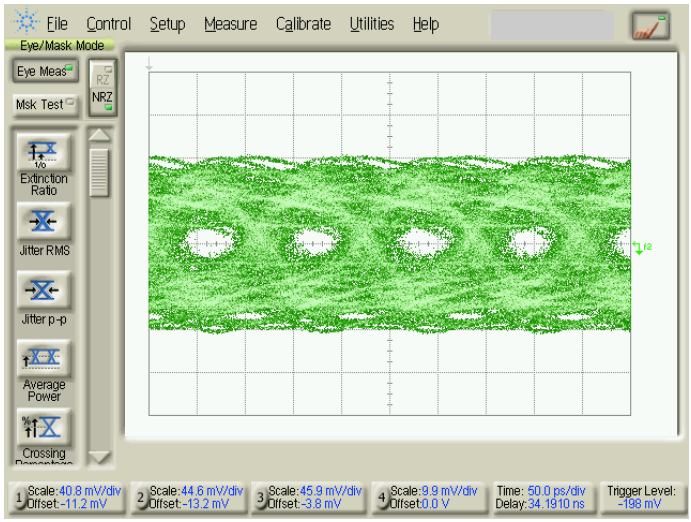


Figure 5.15. Measurement setup of the active delay line equalizer.

A 2^{31}-1 PRBS pattern is generated and transmitted over multimode fiber at 10 Gbps date rate. Figure 5.16 shows the eye diagram of the signal received from the photoreceiver. Figure 5.16 (a) is the signal before the equalization and the Figure 5.16 (b) shows the signal after the equalization. The output voltage level with 50 ohm external termination at the output of the equalizer is 400 mV differential peak-to-peak voltage swing due to the output buffer stage.



(a)



(b)

Figure 5.16. 10 Gbps NRZ signal measurement result before and after the equalizer. (a) 10Gbps NRZ signal eye diagram before the equalization. (b) 10 Gbps NRZ signal eye diagram after the equalization.

The proposed equalizer is fully integrated including all the bias circuit in a standard 0.18 μm CMOS process. Figure 5.17 shows the microphotograph of the fabricated equalizer chip. The overall chip area is 1.15 mm by 0.89 mm including pad area. The power

dissipation, including the single to differential converter and all bias blocks, is 43 mW and 27 mW for output buffer stage.

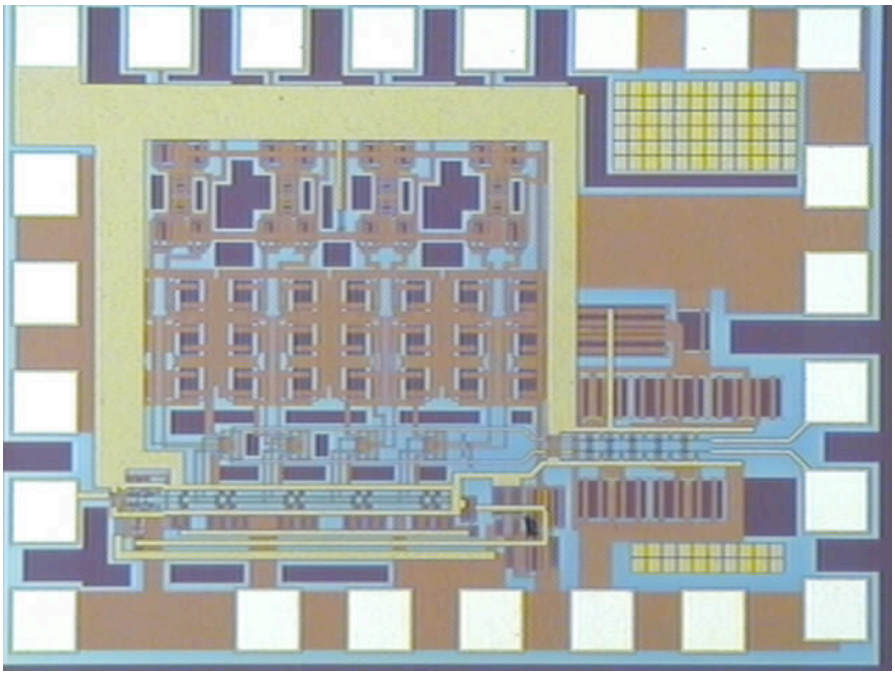


Figure 5.17. Chip picture of the fully integrated equalizer.

In this chapter, the equalizer with an active inductance peaking delay line is presented. The equalizer, additionally features a single to differential converter, a supply noise rejection enhanced bias scheme, and an output buffer fully integrated on one CMOS chip. The equalizer is fabricated in a standard 0.18 μm CMOS process and measured to compensate DMD over the MMF. A 10 Gbps data throughput NRZ signal is transmitted and received through the 500 m of MMF successfully with the developed equalizer.

In the chapter 4 and 5, the equalizer with passive and active tap delay version is presented with the pros and cons of the each approach. In the following chapter, the summary and the future work for the combined digital/wireless optical link and the CMOS based equalization will be shown.

CHAPTER VI

SUMMARY AND FUTURE WORK

The target of this research work is to develop the combined digital/wireless link with the FFE. For the combined optical link module development, new type of combiner is developed on a MLO process developed in Georgia Institute of Technology PRC center. Also the empirical model for the VCSEL is presented in this dissertation. The experimental results by transmitting and receiving the digital baseband signal (OC-48) and the wireless signal (IEEE 802.11a and 802.11b modulation scheme at carrier frequency of 5.8 GHz) are also presented. Finally, to increase further fiber distance, the CMOS based FFE is developed.

This dissertation shows the first 10 Gbps data rate equalizer based on 0.18 μm CMOS technology. First adoption of active inductance load for the tap delay line is described with newly modified Gilbert cell as multiplier for the equalizer. The actual fabrication of the CMOS IC is performed in National Semiconductor Inc. The original contribution of this work is:

1. The first module development for the combined digital/wireless link over the MMF with the VCSEL direct modulation methods.
2. The development of the new type of combiner, which can combine the baseband signal and the selectively chosen wireless signal.

3. The simplified rate-equation based VCSEL model introducing the offset current, which is empirically modeled by the VCSEL injection current.

4. The first 0.18 μm CMOS based equalizer for DMD compensation in MMF at 10 Gbps data throughput.

5. Modified Gilbert-cell structure as a multiplier in the FFE.

6. First use of active inductive peaking delay line for the tap delay in FFE design.

This dissertation began with the introduction of the simultaneous signal transmission over the fiber including the SCM technique. First simultaneous signal transmission via VCSEL direct modulation methods was presented in the chapter 2. For the compact module development, new type of combiner was developed. Different range of frequency was targeted for the combiner design, and the combiner for two different wireless frequency range (i.e. at 5.8 GHz and 14 GHz respectively) was described in this dissertation. The rate-equation based two port VCSEL model was introduced in chapter 2. For the VCSEL model development, several VCSEL measurements were performed. From the DC-IV characteristic, the large signal model for the electrical part of the VCSEL was developed. Also the temperature dependent DC-IV measurement was performed enabling the empirical model of the offset current. The high frequency measurement showed the forward transmission characteristic of the VCSEL enabling the two port VCSEL model. The optical power was modeled by equivalent voltage in VCSEL model. The simultaneous transmission of the OC-48 baseband digital signal and WLAN signal was performed by the developed MLO based module. The experimental result showed the first communication of simultaneous digital/wireless signal with VCSEL direct modulation methods. The experiments were performed with 100 m of

MMF. For the practical implementation, further extension of the MMF distance was required. By this reason, the equalization work was initiated to extend the further bandwidth-distance product of the MMF.

The major signal distortion in MMF is ISI caused by DMD. Therefore, the DMD is characterized by bandwidth-distance product in MMF. In this dissertation, the CMOS based equalizer was developed to further increase the distance of the MMF. Chapter 3 described the background knowledge of the equalization and covers various types of equalizer. From the system level equalizer study, FIR type filter was chosen as an equalizer for the given fiber channel environment over cable equalizer type, because the MMF channel frequency dependent loss characteristic cannot be simply modeled with the high pass filter. Also the receiver side equalizer was selected because the error signal for further adaptive equalization could be acquired easily compared with the transmitter side equalizer. A 500 m of MMF was characterized in frequency domain and converted to the impulse response to extract the optimum tap coefficient values for the equalization. For high-speed operation of the equalizer with a given 0.18 μm CMOS technology, distributed circuit design technique was adopted. The artificial transmission line was implemented with a passive LC network serving as an analog continuous time tap delay line for the equalizer. To overcome the voltage headroom limitation for the conventional Gilbert-cell structure, a modified Gilbert-cell structure was introduced as a multiplier cell in this dissertation. By these efforts, the developed equalizer successfully received the 10 Gbps NRZ data through the 500 m length of MMF, which could obviously extend the distance of MMF in combined digital/wireless link.

Eventhough the advantage of broadband characteristics for the passive LC network approaches, it still has several drawbacks such as consuming large chip space, vulnerable to process variation, and signal insertion loss in the passive LC network. So it is desirable to implement the tap delay line with active devices for practical applications.

Chapter 5 covered the equalizer with active tap delay line and fully integrated features including the single-to-differential converter, noise enhanced bias scheme, and the output buffer stage to transfer the LVDS swing level to external 50 ohm termination. One of the major challenging parts in the active delay line design was to satisfy the required bandwidth for 10 Gbps signal operation. For the broadband circuit design, several circuit topologies were studied in this dissertation. From the literature survey, inductive peaking was chosen as the best candidate for the broadband operation. However inductive peaking technique still requires on-chip inductor, it is desirable to replace the inductors with active components. In this dissertation, the NMOS source follower was used as load with NMOS differential pair to emulate the inductive effect on the desired frequency range, therefore it generated the peaking effect at the edge of 3 dB bandwidth. The simulation results ensured the enhanced bandwidth compared to the differential pair with passive resistive load. Also the adoption of active device for the delay line leaved the feasibility that it could be modified to give variable delay enabling the process independent tap delay. To test the equalizer performance, the optical transceiver with fiber channel was prepared with fabricated equalizer. The 10 Gbps NRZ signal was successfully received after 500 m length of MMF. This is the first 0.18 μm CMOS based equalizer for DMD compensation in MMF at 10 Gbps data rate.

Several future undertakings related to this research is as follows. One of the most obvious research direction is to study the adaptive equalization. The adaptive equalization can be implemented by implementing the LMS algorithm with analog circuit techniques. The error signal for the adaptation can be extracted from the decision circuit at the receiver side. From this observation, it is appropriate research approaches to implement DFE with adaptation.

Another topic to be considered with respect to the equalizer implementation is the adaptation of the delay lock (DLL) loop for the active delay line. As the process variation can shift the ideal amount of delay, it is good research direction to add a DLL and share the delay control signal with equalizer delay line and delay line in DLL. By doing this, the delay in the equalizer is always locked to certain amount of delay supposing the DLL has accurate reference clock. This method will eliminate any process variation effect on the tap delay amount.

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